



Commercial Series CM Radios

Midband (66-88MHz)

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Chapter 1

MODEL CHART AND TECHNICAL SPECIFICATIONS

1.0 CM340/CM360 Model Chart

CM Series Midband 66-88 MHz			
Model			Description
MDM50FNC9AN2_N			CM340 66-88 MHz 1-25W 10-Ch
MDM50FNF9AN2_N			CM360 66-88 MHz 1-25W 100-Ch
		Item	Description
X		FUC1601_	S. Tanapa Midband 25W 10 Ch BNC
	X	FUC1603_	S. Tanapa Midband 25W 100 Ch BNC
X		FCN6288_	Control Head
	X	FCN5523_	Control Head
X	X	HKN4137_	Battery Power Cable
X	X	HMN3596_	Compact Microphone
X	X	GLN7324_	Low Profile Trunnion
X	X	6866546D02_	RTTE Leaflet
X	X	6866537D37_	Safety Leaflet
X		PMUC1033AS	Servicing Kit CM340
	X	FUC1605AS	Servicing Kit CM360

X = Indicates one of each is required

2.0 Technical Specifications

Data is specified for +25°C unless otherwise stated.

General	
Specification	Midband
Frequency Range:	66-88 MHz
Frequency Stability (-30°C to +60°C, 25°C Ref.)	±5 PPM
Channel Capacity:	CM340 - 10 CM360 - 100
Channel Spacing:	12.5/20/25 kHz
Power Output:	1-25W
Power Supply:	13.2Vdc (10.8 - 15.6 Vdc) negative vehicle ground
Dimensions (L X W X H)	118mm X 169mm X 44mm
Weight: Low power (1-25W)	1.02 Kg
Operating Temperature	-30 to 60 ° C
Storage temperature	-40 to 80° C
Shock and Vibration	Meets MIL-STD 810-C,D&E and TIA/EIA 603
Dust	Meets MIL-STD 810-C,D&E and TIA/EIA 603
Humidity	Meets MIL-STD 810-C,D&E and TIA/EIA 603

Transmitter	
Specification	Midband
Frequency Stability:	+/- 5ppm
Modulation Limiting:	±2.5 kHz @ 12.5 kHz ±4.0 kHz @ 20 kHz ±5.0 kHz @ 20/25 kHz
Current Drain Transmit:	8A (25W)
FM Hum and Noise:	-40 dB@12.5 kHz -45 dB@ 20/25 kHz
Conducted/Radiated Emissions:	-36 dBm < 1 GHz -30 dBm > 1 GHz
Adjacent Channel Power	-60dB @12.5, -70dB @ 20/25kHz
Audio Response: (300 to 3000Hz)	+1, -3dB
Audio Distortion: @ 1000 Hz, 60% Rated Maximum Deviation:	3% Typical

Receiver	
Specification	Midband
Sensitivity (12dBSINAD): (ETS)	0.35µV (12.5kHz) 0.30µV (25kHz) Typical
Intermodulation : (ETS)	>65dB
Adjacent Channel Selectivity: (ETS)	70 dB @ 25 kHz 60 dB @ 12.5 kHz
Spurious Rejection: (ETS)	70 dB
Rated Audio: (ETS) (Extended audio with 4 Ohm speaker)	4W Internal , 13W External
Audio Distortion @ Rated Audio:	3% Typical
Hum and Noise:	-40 dB @ 12.5 kHz -45 dB @ 20/25 kHz
Audio Response: (300 to 3000Hz)	+1, -3dB
Conducted Spurious Emission per FCC Part 15:	-57 dBm <1 GHz -47 dBm >1 GHz

*Availability subject to the laws and regulations of individual countries.

THEORY OF OPERATION

1.0 Introduction

This Chapter provides a detailed theory of operation for the Midband circuits in the radio. Details of the theory of operation and trouble shooting for the the associated Controller circuits are included in this Section of the manual.

2.0 Midband (66-88MHz) Receiver

2.1 Receiver Front-End

The received signal from the antenna connector is filtered by the harmonic filter (common to both receive and transmit) and routed to the front end via the antenna switch. The signal is routed to 2-pole pre-selector filter tuned by a dual varacter diode D2301, and on to the LNA, Q2301. This is followed by a 3dB attenuator and a 2-pole post selector filter, tuned by varactor D2304. The varactor control voltage is generated by a DAC in the ASFIC (U504-6). An inverting op-amp stage (U517) amplifies the control signal to provide 0-8V. Signal RX_FE_TUNE voltage is increased under software control for higher receive frequencies. Note that the same DAC is used to control the transmitter power. The 9V supply to the LNA (Q2301) is turned on by Q4 when RX_EN is high. Q2302 controls the biasing so that Q2301 is operated with a constant collector current (15mA).

In Local Mode, attenuator R38 improves the intermodulation performance prior to the first mixer. In Distance Mode, normal operation, R38 is bypassed by diode D1, which is forward biased by Q1 turning on when the LOC_DIST line from the microprocessor (U403-45) is high.

The first mixer is a passive, double-balanced type, consisting of T1, T2 and U1. This mixer provides all of the necessary rejection of the half-IF spurious response. High-side injection at +15 dBm is delivered to the first mixer. The mixer output is then connected to a duplex network which matches its output to the XTAL filter input (FL2201) at the IF frequency of 21.4 MHz. The duplex network terminates into a 50 ohm resistor (R41) at all other frequencies.

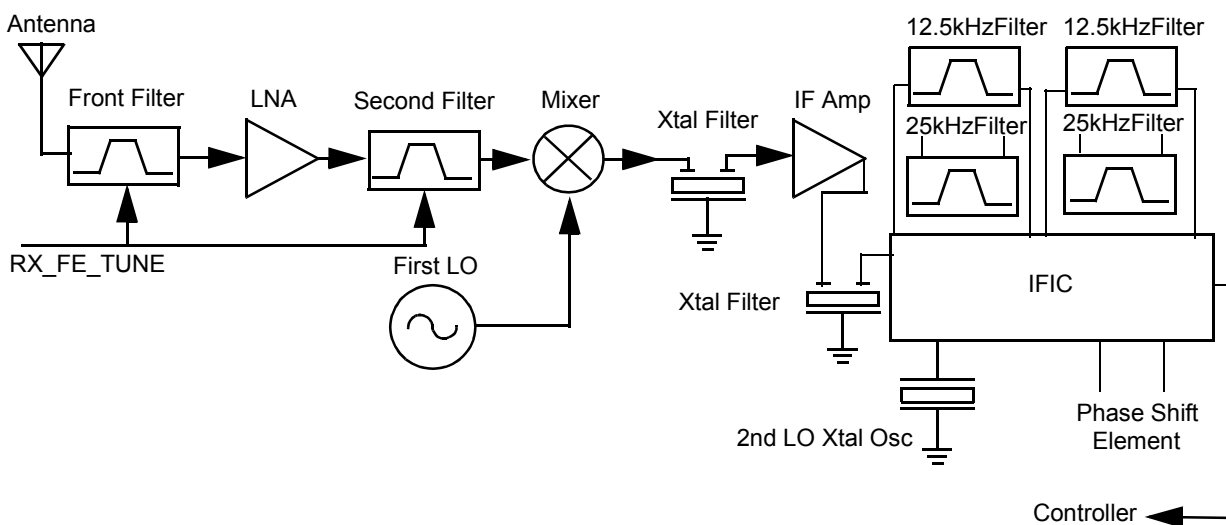


Figure 2-1 Midband Receiver Block Diagram

2.2 Receiver Back End

The IF signal from the crystal filter enters the IF amplifier which provides 20 dB of gain and feeds the IF IC (U2) at pin 1. The first IF signal at 21.4 MHz mixes with the second local oscillator (LO) at 20.945 MHz to produce the second IF at 455 kHz. The second LO uses the external crystal Y2. The second IF signal is amplified and filtered by two external ceramic filters (FL4/FL3 for 12.5KHz channel spacing and FL5/FL2 for 25KHz channel spacing). The IF IC demodulates the signal by means of a quadrature detector and feeds the detected audio (via pin 7) to the audio processing circuits. At IF IC pin 5, an RSSI signal is available with a dynamic range of 70 dB.

3.0 Midband Transmitter Power Amplifier (66-88 MHz)

The radio's 25W PA is a three-stage amplifier used to amplify the output from the TX_INJ to the antenna port. All three stages utilize LDMOS technology. The gain of the first stage (U101) and the second stage (Q105) is adjustable and is controlled by pin 7 of U103-2 via U103-3 and U102-1. It is followed by an LDMOS final stage Q100.

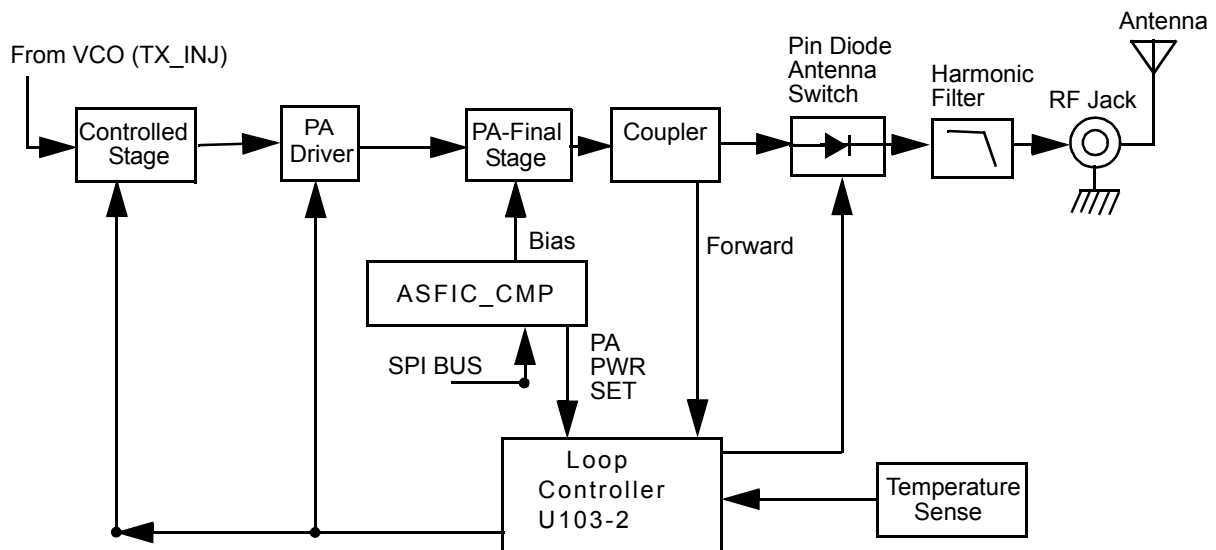


Figure 2-2 Midband Transmitter Block Diagram

Devices U101, Q105 and Q100 are surface mounted. When assembled, Q100 is in direct contact with the chassis. Heat spreader M105 ensures good thermal contact for Q105.

3.1 First Power Controller Stage

The first stage (U101) is a variable gain integrated circuit containing two LDMOS FET amplifier stages which can provide up to 20dB gain. It amplifies the RF signal from the VCO (TX_INJ). The output power of stage U101 is controlled by a DC voltage applied to pin 1 from the op-amp U103-3, pin 8. The control voltage simultaneously varies the bias of two FET stages within U101. This biasing point determines the overall gain of U101 and therefore its output drive level to Q105, which in turn controls the output power of the PA.

For a given control voltage input on VCNTR1, Op-amp U103-3 monitors the drain current of U101 via resistor R122 and adjusts the bias voltage of U101 accordingly.

In receive mode, the DC voltage from RX_EN line turns on Q101, grounding VCNTR1, which in turn switches off the biasing voltage to U101.

3.2 Power Controlled Driver Stage

The next stage is an LDMOS device (Q105) which provides a gain of up to 15dB. This device requires a positive gate bias and a quiescent current flow for proper operation. The bias is set during transmit mode by the drain current control op-amp U102-1, and fed to the gate of Q105 via the resistive network (R175, R147, R178, R179).

For a given control voltage input on VCNTR2, Op-amp U102-1 monitors the drain current of Q105 via resistors R126-7 and adjusts the bias voltage of Q105 so that the current remains constant.

In receive mode the DC voltage from RX_EN line turns on Q102, grounding VCNTR1, which in turn switches off the biasing voltage to Q105.

3.3 Final Stage

The final stage is an LDMOS device (Q100) providing a gain of 12dB. This device also requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line PA_BIAS is set in transmit mode by the ASFIC and fed to the gate of Q100 via the resistive network R134, R131. This bias voltage is tuned in the factory. If the transistor is replaced, the bias voltage must be tuned using the Tuner. Care must be taken not to damage the device by exceeding the maximum allowed bias voltage. The device's drain current is drawn directly from the radio's DC supply voltage input, B+, via L117 and L115.

The output matching network transforms the impedance to 50 ohms and feeds the directional coupler.

3.4 Bi-Directional Coupler

The bi-directional Coupler is a microstrip printed circuit, which couples a small amount of the forward and reverse power of the RF power from Q100. The coupled signal is rectified to an output power which is proportional to the DC voltage rectified by diode D105; and the resulting DC voltage is routed to the power control section to ensure that the forward power out of the radio is held to a constant value.

3.5 Antenna Switch

The antenna switch utilizes the existing dc feed (B+) to the last stage device (Q100). In transmit mode, both PIN diodes (D103, D104) are forward biased. This is achieved by pulling down the voltage at the cathode end of D104 to around 12.4V (0.7V drop across each diode). The current through the diodes needs to be set at around 100 mA to fully open the transmit path through resistor R108. Q106 is a current source controlled by Q103 which is turned on in Tx mode by TX_EN. VR102 ensures that the voltage at resistor R107 never exceeds 5.6V, limiting the current to approximately 100mA.

3.6 Harmonic Filter

Inductors L1511, L1512, L1513 and L1515 along with capacitors C1518 to C1523, C1528, C1532 to C1535, C1537 to C1539 and C1542 form a 9-element elliptical low-pass filter to attenuate harmonic energy coming from the transmitter. Resistor R152 drains any electrostatic charges that might otherwise build up on the antenna. The harmonic filter also prevents high level RF signals above the receiver passband from reaching the receiver circuits to improve spurious response rejection.

3.7 Power Control

The output power is regulated by using a forward power detection control loop. A directional coupler samples a portion of the forward and reflected RF power. The forward sampled RF is rectified by diode D105, and the resulting DC voltage is routed to the operational amplifier U100. The error output current is then routed to an integrator, and converted into the control voltage. This voltage controls the bias of the pre-driver (U101) and driver (Q105) stages. The output power level is set by way of a DAC, PWR_SET, in the ASFIC (U504), which acts as the forward power control loop reference.

The sampled reflected power is rectified by diode D107, The resulting DC voltage is amplified by an operational amplifier U100 and routed to the summing junction. This detector protects the final stage Q100 from reflected power by increasing the error current. The temperature sensor protects the final stage Q100 from overheating by increasing the error current. A thermistor RT100 measures the final stage Q100 temperature. The voltage divider output is routed to an operational amplifier U103 and then goes to the summing junction. The Zener Diode VR101 keeps the loop control voltage below 5.6V and eliminates the DC current from the 9.3 regulator U501.

Two local loops for the Pre Driver (U101) and for the Driver (Q105) are used in order to stabilize the current for each stage.

In Rx mode, the two transistors Q101 and Q102 go to saturation and shut down the transmitter by applying ground to the Pre Driver U101 and for the Driver Q105 control.

VR103, VR104 and Q104, Q108, Q109 and associated circuitry provide protection during load dump transients.

4.0 Midband (66-88MHz) Frequency Synthesis

The synthesizer consists of a reference oscillator (Y202), low voltage Fractional-N (LVFRAC-N) synthesizer (U200), and a voltage controlled oscillator (VCO) (Q2741/Q2751).

4.1 Reference Oscillator

The reference oscillator is a crystal (Y202) controlled Colpitts oscillator and has a frequency of 16.8MHz. The oscillator transistor and start-up circuit are located in the LVFRAC-N (U200) while the oscillator feedback capacitors, crystal, and tuning varactors are external. An analog-to-digital (A/D) converter internal to the LVFRAC-N (U200) and controlled by the microprocessor via SPI sets the voltage at the warp output of U200 pin 25. This sets the frequency of the oscillator. Consequently, the output of the crystal Y202 is applied to U200 pin 23.

The method of temperature compensation is to apply an inverse Bechmann voltage curve, which matches the crystal’s Bechmann curve to a varactor that constantly shifts the oscillator back on frequency. The crystal vendor characterizes the crystal over a specified temperature range and codes this information into a bar code that is printed on the crystal package. In production, this crystal code is read via a 2-dimensional bar code reader and the parameters are saved.

This oscillator is temperature compensated to an accuracy of +/-2.5 PPM from -30 to 60 degrees C. The temperature compensation scheme is implemented by an algorithm that uses five crystal parameters (four characterize the inverse Bechmann voltage curve and one for frequency accuracy of the reference oscillator at 25 degrees C). This algorithm is implemented by the LVFRAC-N (U200) at the power up of the radio.

4.2 Fractional-N Synthesizer

The LVFRAC-N U200 consists of a pre-scaler, programmable loop divider, control divider logic, phase detector, charge pump, A/D converter for low frequency digital modulation, balanced attenuator used to balance the high and low frequency analog modulation, 13V positive voltage multiplier, serial interface for control, and a super filter for the regulated 9 volts.

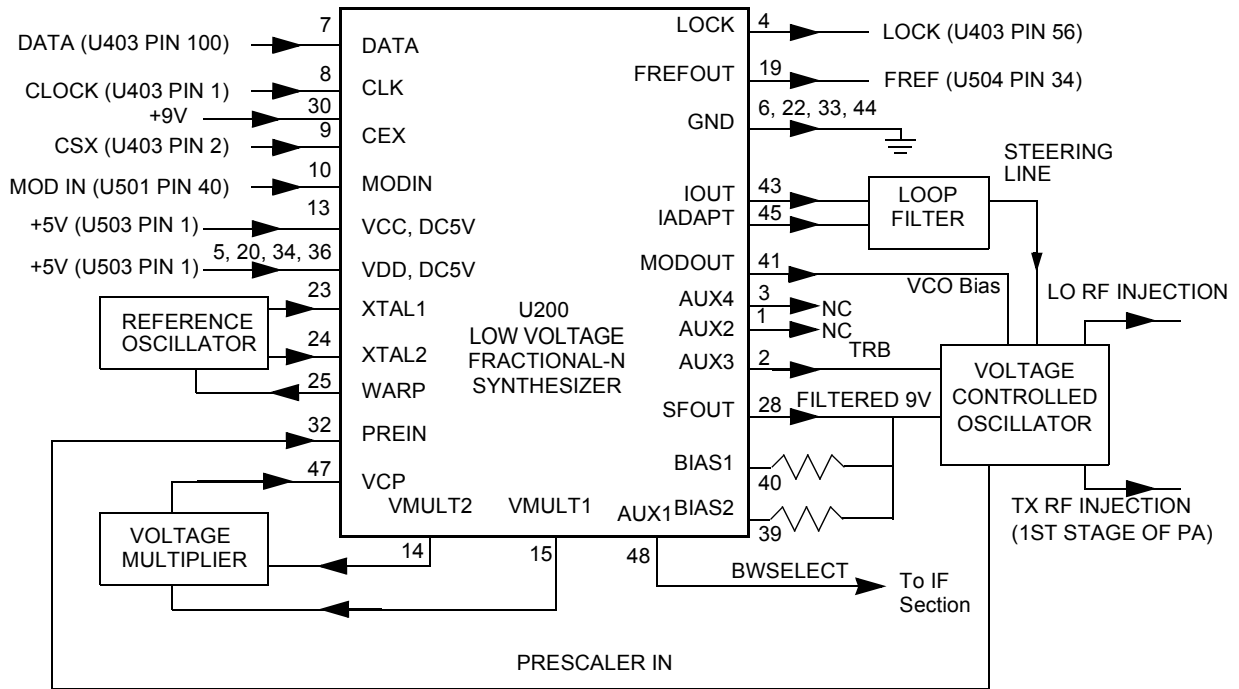


Figure 2-3 Midband Synthesizer Block Diagram

A voltage of 9.3V applied to the super filter input (U200, pin 30) supplies an output voltage of 8.6Vdc (VSF) at U200, pin 28. This supplies 8.6 V to the two VCO circuits.

To generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U200, pin 47) while using a low voltage 5Vdc supply, a 13V positive voltage multiplier is used (D200, D201, and capacitors C2024, 2025, 2026, 2055, 2027, 2001).

Output lock (U200, pin 4) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. A 16.8 MHz reference frequency is provided at U200, pin 19.

4.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) uses 2 colpitts oscillators, FET Q2741 for transmit and FET Q2751 for receive. The appropriate oscillator is switched on or off by LVFRAC-N IC output AUX3 (U200-2) using transistors Q2742 and Q2752. In RX mode AUX3 is nearly at ground level and Q2742 enables a current flow from the source of FET Q2751 while Q2752 is switched off. In TX mode AUX3 is about 3.3V DC and Q2742 is switched off. Q2752 is switched on and enables a current flow from the source of FET Q2741 while Q2751 is switched off. When switched on the FETs draw a drain current of 8 mA from the LVFRAC-N IC super filter output. The frequency of the receive oscillator is mainly determined by L2752, L2753, C2752 - C2756 and varactor diodes D2751 / D2752. Diode D2754 controls the amplitude of the oscillator. The frequency of the transmit oscillator is mainly determined by L2734, C2736 - C2740 and varactor diodes D2732 / D2733. Diode D2739 controls the amplitude of the oscillator. With a steering voltage from 3V to 10V at the varactor diodes the RX frequency range from 87.4 MHz to 109.4 MHz and the TX frequency range from 66 MHz to 88 MHz are covered. In TX mode the modulation signal coming from the LVFRAC-N synthesizer IC (U200 pin 41) modulates the TX VCO via varactor diode D2731.

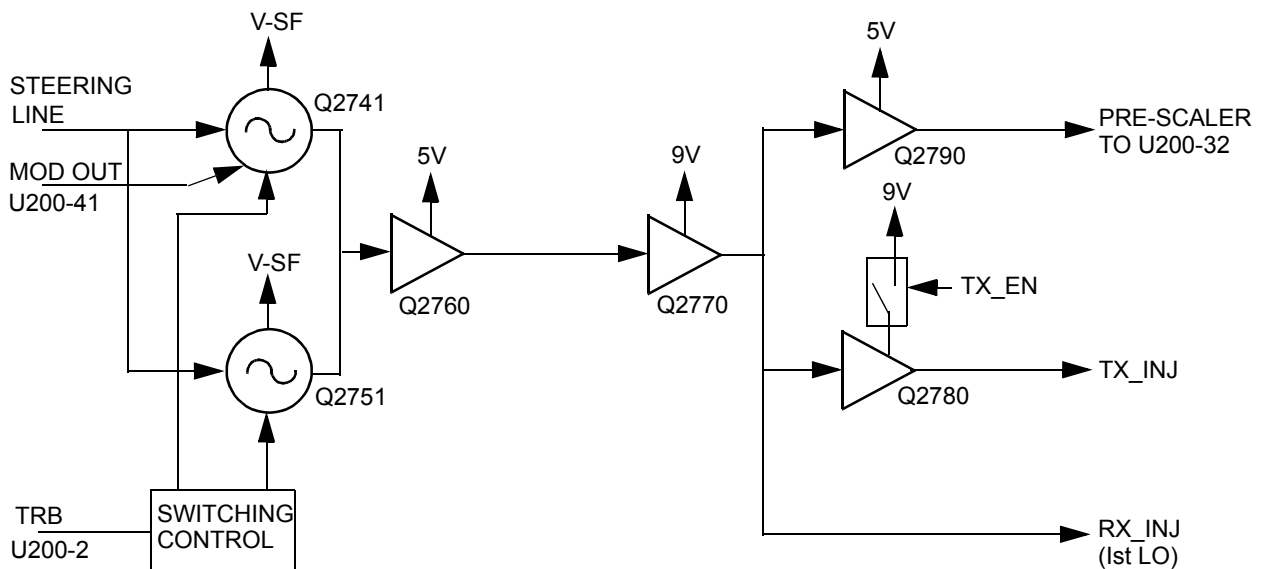


Figure 2-4 Midband VCO Block Diagram

Both oscillator outputs are combined and buffered by the VCO Buffer Q2760. Q2760 draws a collector current of 13 mA from the stabilized 5V and drives the Mixer Buffer Q2770. Q2770 draws a collector current of 19 mA from the 9V3 voltage and drives the PA Buffer Q2780 (Pout = 13dBm) and the Pre-scaler Buffer Q2790. Q2790 draws a collector current of 8 mA from the stabilized 5V and drives the pre-scaler internal to the LVFRAC-N IC. In transmit mode, the 9.3V supply for the TX PA Buffer Q2780, is turned on by Q2791. PA Buffer Q2780 draws a collector current of 19mA. The injection signal RX_INJ with a level of 10dBm feeds the mixer through R2774. The buffer stages Q2760, Q2770, Q2780 and the feedback amplifier Q2790 provide the necessary gain and isolation for the synthesizer loop.

4.4 Synthesizer Operation

The synthesizer consists of a low voltage FRAC-N IC (LVFRAC-N), reference oscillator, charge pump circuits, loop filter circuit, and DC supply. The output from the pre-scaler buffer (Q2790) is fed to the PREIN, pin 32 of U200 via a low pass filter which attenuates harmonics and provides a correct input level to the LVFRAC-N in order to close the synthesizer loop.

The pre-scaler in the synthesizer (U200) is a dual modulus pre-scaler with selectable divider ratios. The divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SPI. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider's output signal with the reference signal. The reference signal is generated by dividing down the signal of the reference oscillator (Y202).

The output signal of the phase detector is a pulsed dc signal that is routed to the charge pump. The charge pump outputs a current from U200, pin 43 (IOUT). The loop filter (consisting of R224, R217, R234, C2074, C2078, C2028, and L205) transforms this current into a voltage that is applied to the varactor diodes D2751, D2752 for Rx and D2732, D2733 for Tx. The output frequency is determined by this control voltage. The current can be set to a value fixed in the LVFRAC-N or to a value determined by the currents flowing into BIAS 1 (U200, pin 40) or BIAS 2 (U200, pin 39). The currents are set by the value of R200 or R206 respectively. The selection of the three different bias sources is done by software programming.

To modulate the synthesizer loop, a two-spot modulation method is utilized via the MODIN (U200, pin 10) input of the LVFRAC-N. The audio signal is applied to both the A/D converter (low frequency path) and the balance attenuator (high frequency path). The A/D converter converts the low frequency analog modulating signal into a digital code which is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is presented at the MODOUT port of the LVFRAC-N (U200 pin 41) and connected to the VCO modulation varactor D2731.

5.0 Controller Theory of Operation

This section provides a detailed theory of operation for the radio and its components. The main radio is a single-board design, consisting of the transmitter, receiver, and controller circuits. A control head is connected by an extension cable. The control head contains LED indicators, a microphone connector, buttons, and speaker.

In addition to the power cable and antenna cable, an accessory cable can be attached to a connector on the rear of the radio. The accessory cable enables you to connect accessories to the radio, such as an external speaker, emergency switch, foot-operated PTT, and ignition sensing, etc.

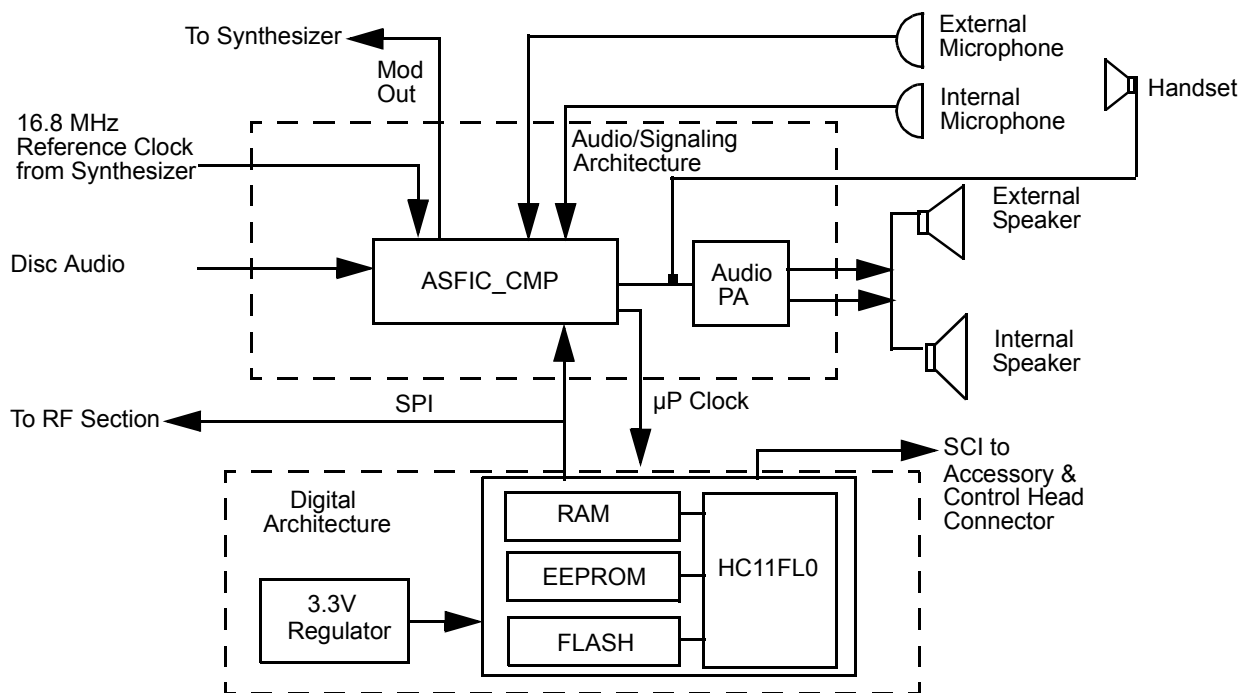


Figure 2-5 Controller Block Diagram

5.1 Radio Power Distribution

Voltage distribution is provided by five separate devices:

- U514 P-cH FET - Batt + (Ext_SWB+)
- U501 LM2941T - 9.3V
- U503 LP2951CM - 5V
- U508 MC 33269DTRK - 3.3V
- U510 LP2986ILDY - 3.3V Digital

The DC voltage applied to connector P2 supplies power directly to the following circuitry:

- Electronic on/off control
- RF power amplifier
- 12 volts P-cH FET -U514
- 9.3 volt regulator
- Audio PA

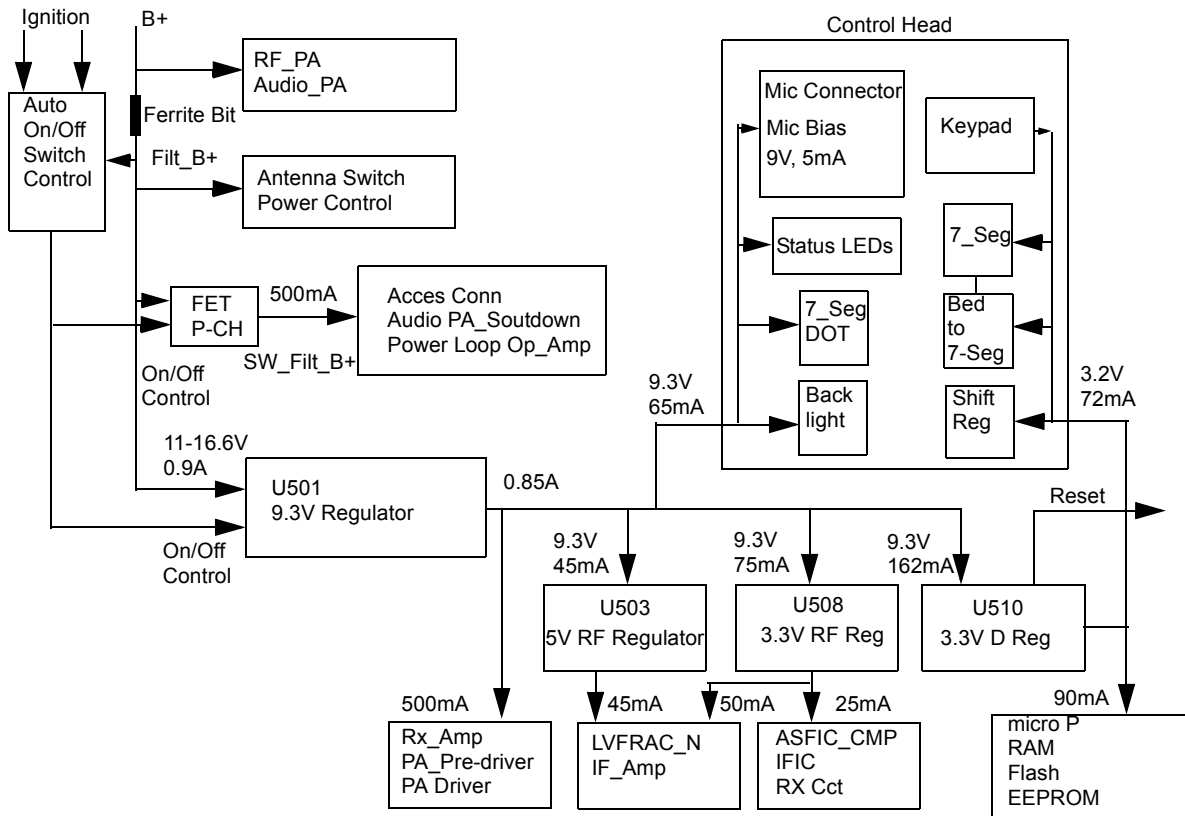


Figure 2-6 DC Power Distribution Block Diagram

Regulator U501 is used to generate the 9.3 volts required by some audio circuits, the RF circuitry and power control circuitry. Input and output capacitors are used to reduce high frequency noise. Resistors R5001 / R5081 set the output voltage of the regulator. This regulator output is electronically enabled by a 0 volt signal on pin 2. Q502, Q505 and R5038 are used to disable the regulator when the radio is turned off.

Voltage regulator U510 provides 3.3 volts for the digital circuitry. Operating voltage is from the regulated 9.3V supply. Input and output capacitors are used to reduce high frequency noise and provide proper operation during battery transients. U510 provides a reset output that goes to 0 volts if the regulator output goes below 3.1 volts. This is used to reset the controller to prevent improper operation.

Voltage regulator U508 provides 3.3V for the RF circuits and ASFIC_CMP. Input and output capacitors are used to reduce the high frequency noise and provide proper operation during battery transients.

Voltage regulator U503 provides 5V for the RF circuits. Input and output capacitors are used to reduce the high frequency noise and provide proper operation during battery transients.

VSTBY is used only for CM360 5-tone radios.

The voltage VSTBY, which is derived directly from the supply voltage by components R5103 and VR502, is used to buffer the internal RAM. Capacitor C5120 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Dual diode D501 prevents radio circuitry from discharging this capacitor. When the supply voltage is applied to the radio, C5120 is charged via R5103 and D501.

5.2 Protection Devices

Diode VR500 acts as protection against ESD, wrong polarity of the supply voltage, and load dump. VR692 - VR699 are for ESD protection.

5.3 Automatic On/Off

The radio can be switched ON in any one of the following ways:

- On/Off switch. (No Ignition Mode)
- Ignition and On/Off switch (Ignition Mode)
- Emergency

5.3.1 No Ignition Mode

When the radio is connected to the car battery for the first time, Q500 will be in saturation, Q503 will cut-off, Filt_B+ will pass through R5073, D500, and S5010-pin 6 (On/Off switch). When S5010 is ON, Filt_B+ will pass through S5010-pin5, D511, R5069, R5037 and base of Q505 and move Q505 into saturation. This pulls U501-pin2 through R5038, D502 to 0.2V and turns On U514 and U501 9.3V regulator which supplies voltage to all other regulators and consequently turns the radio on, When U504 (ASFIC_CMP) gets 3.3V, GCB2 goes to 3.3V and holds Q505 in saturation, for soft turn off.

5.3.2 Ignition Mode

When ignition is connected for the first time, it will force high current through Q500 collector, This will move Q500 out of saturation and consequently Q503 will cut-off. S5010 pin 6 will get ignition voltage through R601 (for load dump), R610, (R610 & C678 are for ESD protection), VR501, R5074, and D500. When S5010 is ON, Filt_B+ passes through S5010-pin 5, D511, R5069, R5037 and base of Q505 and inserts Q505 into saturation. This pulls U501-pin 2 through R5038, D502 to 0.2V and turns on U514 and U501 9.3V regulator which supply voltage to all other regulators and turns the radio on, When U504 (ASFIC_CMP) get 3.3V supply, GCB2 goes to 3.3V and holds Q505 in saturation state to allow soft turn off,

When ignition is off Q500, Q503 will stay at the same state so S5010 pin 6 will get 0V from Ignition, Q504 goes from Sat to Cut, ONOFF_SENSE goes to 3.3V and it indicates to the radio to soft turn itself by changing GCB2 to '0' after de registration if necessary.

5.3.3 Emergency Mode

The emergency switch (P1 pin 9), when engaged, grounds the base of Q506 via EMERGENCY_ACCES_CONN. This switches Q506 to off and consequently resistor R5020 pulls the collector of Q506 and the base of Q506 to levels above 2 volts. Transistor Q502 switches on and pulls U501 pin2 to ground level, thus turning ON the radio. When the emergency switch is released R5030 pulls the base of Q506 up to 0.6 volts. This causes the collector of transistor Q506 to go low (0.2V), thereby switching Q502 to off.

While the radio is switched on, the μ P monitors the voltage at the emergency input on the accessory connector via U403-pin 62. Three different conditions are distinguished: no emergency kit is connected, emergency kit connected (unpressed), and emergency press.

If no emergency switch is connected or the connection to the emergency switch is broken, the resistive divider R5030 / R5049 will set the voltage to about 3.14 volts (indicates no emergency kit found via EMERGENCY_SENSE line). If an emergency switch is connected, a resistor to ground within the emergency switch will reduce the voltage on EMERGENCY_SENSE line, and indicate to the μ P that the emergency switch is operational. An engaged emergency switch pulls line EMERGENCY_SENSE line to ground level. Diode VR503 limits the voltage to protect the μ P input.

While EMERGENCY_ACCES_CONN is low, the μ P starts execution, reads that the emergency input is active through the voltage level of μ P pin 64, and sets the DC POWER ON output of the ASFIC CMP pin 13 to a logic high. This high will keep Q505 in saturation for soft turn off.

5.4 Microprocessor Clock Synthesiser

The clock source for the μ P system is generated by the ASFIC CMP (U504). Upon power-up the synthesizer IC (FRAC-N) generates a 16.8 MHz waveform that is routed from the RF section to the ASFIC CMP pin 34. For the main board controller the ASFIC CMP uses 16.8 MHz as a reference input clock signal for its internal synthesizer. The ASFIC CMP, in addition to audio circuitry, has a programmable synthesizer which can generate a synthesized signal ranging from 1200Hz to 32.769MHz in 1200Hz steps.

When power is first applied, the ASFIC CMP will generate its default 3.6864MHz CMOS square wave UP CLK (on U504 pin 28) and this is routed to the μ P (U403 pin 90). After the μ P starts operation, it reprograms the ASFIC CMP clock synthesizer to a higher UP CLK frequency (usually 7.3728 or 14.7456 MHz) and continues operation.

The ASFIC CMP may be reprogrammed to change the clock synthesizer frequencies at various times depending on the software features that are executing. In addition, the clock frequency of the synthesizer is changed in small amounts if there is a possibility of harmonics of the clock source interfering with the desired radio receive frequency.

The ASFIC CMP synthesizer loop uses C5025, C5024 and R5033 to set the switching time and jitter of the clock output. If the synthesizer cannot generate the required clock frequency it will switch back to its default 3.6864MHz output.

Because the ASFIC CMP synthesizer and the μ P system will not operate without the 16.8 MHz reference clock it (and the voltage regulators) should be checked first when debugging the system.

5.5 Serial Peripheral Interface (SPI)

The μ P communicates to many of the IC's through its SPI port. This port consists of SPI TRANSMIT DATA (MOSI) (U403-pin100), SPI RECEIVE DATA (MISO) (U403-pin 99), SPI CLK (U0403-pin1) and chip select lines going to the various IC's, connected on the SPI PORT (BUS). This BUS is a synchronous bus, in that the timing clock signal CLK is sent while SPI data (SPI TRANSMIT DATA or SPI RECEIVE DATA) is sent. Therefore, whenever there is activity on either SPI TRANSMIT DATA or SPI RECEIVE DATA there should be a uniform signal on CLK. The SPI TRANSMIT DATA is used to send serial from a μ P to a device, and SPI RECEIVE DATA is used to send data from a device to a μ P.

There are two IC's on the SPI BUS, ASFIC CMP (U504 pin 22)), and EEPROM (U400). In the RF sections there is one IC on the SPI BUS, the FRAC-N Synthesizer. The chip select line CSX from U403 pin 2 is shared by the ASFIC CMP and FRAC-N Synthesizer. Each of these IC's check the SPI data and when the sent address information matches the IC's address, the following data is processed.

When the μ P needs to program any of these Is it brings the chip select line CSX to a logic "0" and then sends the proper data and clock signals. The amount of data sent to the various IC's are different; e.g., the ASFIC CMP can receive up to 19 bytes (152 bits). After the data has been sent the chip select line is returned to logic "1".

5.6 SBEP Serial Interface

The SBEP serial interface allows the radio to communicate with the Customer Programming Software (CPS), or the Universal Tuner via the Radio Interface Box (RIB) or the cable with internal RIB. This interface connects to the SCI pin via control head connector (J2-pin 17) and to the accessory connector P1-6 and comprises BUS+. The line is bi-directional, meaning that either the radio or the RIB can drive the line. The μ P sends serial data and it reads serial data via pin 97. Whenever the μ P detects activity on the BUS+ line, it starts communication.

5.7 General Purpose Input/Output

The controller provides six general purpose lines (PROG I/O) available on the accessory connector P1 to interface to external options. Lines PROG IN 3 and 6 are inputs, PROG OUT 4 is an output and PROG IN OUT 8, 12 and 14 are bi-directional. The software and the hardware configuration of the radio model define the function of each port.

- PROG IN 3 can be used as external PTT input, or others, set by the CPS. The μ P reads this port via pin 72 and Q412.
- PROG OUT 4 can be used as external alarm output, set by the CPS. Transistor Q401 is controlled by the μ P (U403 pin 55)
- PROG IN 6 can be used as normal input, set by the CPS. The μ P reads this port via pin 73 and Q411. This pin is also used to communicate with the RIB if resistor R421 is placed.
- DIG IN OUT 8,12,14 are bi-directional and use the same circuit configuration. Each port uses an output Q416, Q404, Q405 controlled by μ P pins 52, 53, 54. The input ports are read through μ P pins 74, 76, 77; using Q409, Q410, Q411

5.8 Normal Microprocessor Operation

For this radio, the μP is configured to operate in one of two modes, expanded and bootstrap. In expanded mode the μP uses external memory devices to operate, whereas in bootstrap operation the μP uses only its internal memory. In normal operation of the radio the μP is operating in expanded mode as described below.

During normal operation, the μP (U403) is operating in expanded mode and has access to 3 external memory devices; U400 (EEPROM), U402 (SRAM), U404 (Flash). Also, within the μP there are 3 Kilobytes of internal RAM, as well as logic to select external memory devices.

The external EEPROM (U400) space contains the information in the radio which is customer specific, referred to as the codeplug. This information consists of items such as: 1) what band the radio operates in, 2) what frequencies are assigned to what channel, and 3) tuning information.

The external SRAM (U402) as well as the μP 's own internal RAM space are used for temporary calculations required by the software during execution. All of the data stored in both of these locations is lost when the radio powers off.

The μP provides an address bus of 16 address lines (ADDR 0 - ADDR 15), and a data bus of 8 data lines (DATA 0 - DATA 7). There are also 3 control lines; CSPROG (U403-38) to chip select U404-pin 30 (FLASH), CSGP2 (U403-pin 41) to chip select U404-pin 20 (SRAM) and PG7_R_W (U403-pin 4) to select whether to read or to write. The external EEPROM (U400-pin1).

When the μP is functioning normally, the address and data lines should be toggling at CMOS logic levels. Specifically, the logic high levels should be between 3.1 and 3.3V, and the logic low levels should be between 0 and 0.2V. No other intermediate levels should be observed, and the rise and fall times should be $<30\text{ns}$.

The low-order address lines (ADDR 0 - ADDR 7) and the data lines (DATA 0-DATA 7) should be toggling at a high rate, e.g., you should set your oscilloscope sweep to $1\mu\text{s}/\text{div}$. or faster to observe individual pulses. High speed CMOS transitions should also be observed on the μP control lines.

On the μP the lines XIRQ (U403-pin 48), MODA LIR (U403-pin 58), MODB VSTPY (U403-pin 57) and RESET (U403-pin 94) should be high at all times during normal operation. Whenever a data or address line becomes open or shorted to an adjacent line, a common symptom is that the RESET line goes low periodically, with the period being in the order of 20ms. In the case of shorted lines you may also detect the line periodically at an intermediate level, i.e. around 2.5V when two shorted lines attempt to drive to opposite rails.

The MODA LIR (U403-pin 58) and MODB VSTPY (U403-pin 57) inputs to the μP must be at a logic "1" for it to start executing correctly. After the μP starts execution it will periodically pulse these lines to determine the desired operating mode. While the Central Processing Unit (CPU) is running, MODA LIR is an open-drain CMOS output which goes low whenever the μP begins a new instruction. An instruction typically requires 2-4 external bus cycles, or memory fetches.

There are eight analog-to-digital converter ports (A/D) on U403 labelled within the device block as PEO-PE7. These lines sense the voltage level ranging from 0 to 3.3V of the input line and convert that level to a number ranging from 0 to 255 which is read by the software to take appropriate action.

5.9 Static Random Access Memory (SRAM)

The SRAM (U402) contains temporary radio calculations or parameters that can change very frequently, and which are generated and stored by the software during its normal operation. The information is lost when the radio is turned off.

The device allows an unlimited number of write cycles. SRAM accesses are indicated by the CS signal U402 (which comes from U403-CSGP2) going low. U402 is commonly referred to as the external RAM as opposed to the internal RAM which is the 3 Kilobytes of RAM which is part of the 68HC11FLO. Both RAM spaces serve the purpose. However, the internal RAM is used for the calculated values which are accessed most often.

Capacitor C402 and C411 serves to filter out any AC noise which may ride on +3.3 V at U402

6.0 Control Board Audio and Signalling Circuits

6.1 Audio Signalling Filter IC and Compander (ASFIC CMP)

The ASFIC CMP (U504) used in the controller has the following four functions:

1. RX/TX audio shaping, i.e. filtering, amplification, attenuation
2. RX/TX signaling, PL/DPL/HST/MDC
3. Squelch detection
4. μ P clock signal generation

The ASFIC CMP is programmable through the SPI BUS (U504 pins-20/21/22), normally receiving 19 bytes. This programming sets up various paths within the ASFIC CMP to route audio and/or signaling signals through the appropriate filtering, gain and attenuator blocks. The ASFIC CMP also has 6 General Control Bits GCB0-5 which are CMOS level outputs and used for the following:

- GCB0 - BW Select
- GCB1 - switches the audio PA On/Off
- GCB2 - DC Power On switches the voltage regulator (and the radio) on and off
- GCB3 - Control on MUX U509 pin 9 to select between Low Cost Mic path to STD Mic Path
- GCB4 - Control on MUX U509 pin 11 to select between Flat RX path to filtered RX path on the accessory connector.
- GCB5 - Control on MUX U509 pin 10 to select between Flat TX path mute and Flat TX path

7.0 Transmit Audio Circuits

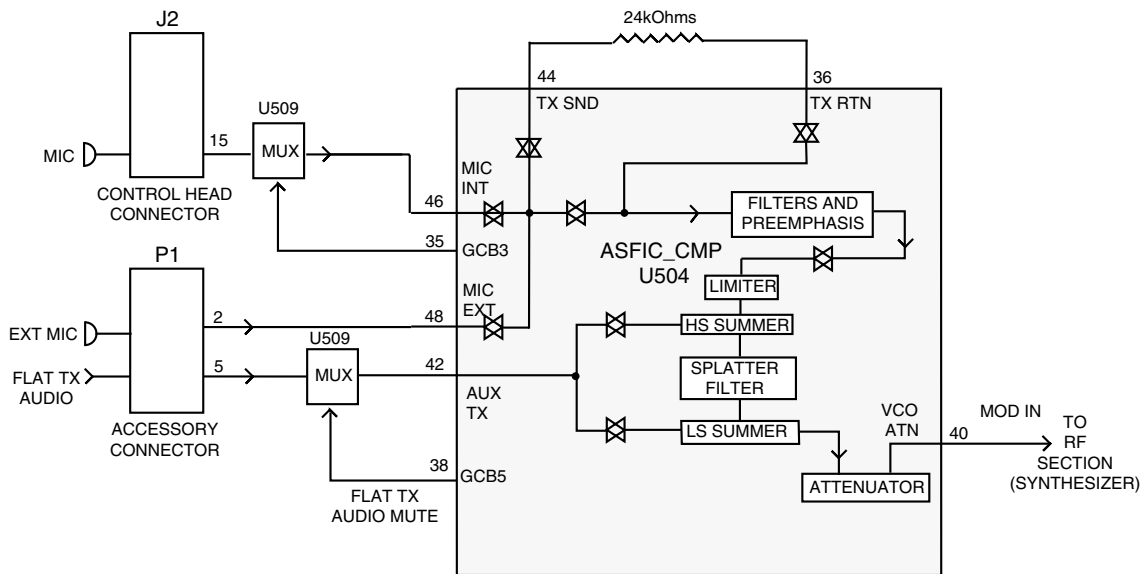


Figure 2-7 Transmit Audio Paths

7.1 Microphone Input Path

The radio supports 2 distinct microphone paths known as internal (from control head J2-15) and external mic (from accessory connector P1-2) and an auxiliary path (FLAT TX AUDIO, from accessory connector P1-5). The microphones used for the radio require a DC biasing voltage provided by a resistive network.

The two microphone audio input paths enter the ASFIC CMP at U504-pin 48 (external mic) and U504-pin 46 (internal mic). The microphone is plugged into the radio control head and connected to the audio DC via J2-pin 15. The signal is then routed via C5045 to MUX U509 that select between two paths with different gain to support Low Cost Mic (Mic with out amplifier in it) and Standard Mic.

7.1.1 Low Cost Microphone

Hook Pin is shorted to Pin 1(9.3V) inside the Low Cost Mic, This routes 9.3V to R429, and creates 2.6V on MIC_SENSE (u.P U403-67) by Voltage Divider R429/R430. U403 senses this voltage and sends command to ASFIC_CMP U504 to get GCB3 = '0'. The audio signal is routed from C5045 via U509-5 (Z0), R5072, U507, R5026, C5091, R5014 via C5046 to U504- 46 int. mic (C5046 100nF creates a 159Hz pole with U504- 46 int mic impedance of 16Kohm).

7.1.2 Standard Microphone

Hook Pin is shorted to the hook mic inside the standard Mic, If the mic is out off hook, 3.3V is routed to R429 via R458, D401, and it create 0.7V on MIC_SENSE (u.P U403-67) by Voltage Divider R429/R430. U403 senses this voltage and sends command to ASFIC_CMP U504 to get GCB3 = '1'. The audio signal is routed from C5045 via U509-3 (Z1), R5072, U507, R5026, C5091, R5014 via C5046 to U504- 46 int mic (C5046 100nF create a159Hz pole with U504- 46 int mic impedance of 16Kohm). 9.3VDC is routed via R5077, R5075 to J2-15, It create 4.65V with Mic Impedance. C5010 supplies AC Ground to create AC impedance of 510 Ohms via R5075. and Filter 9.3V DC mic bias supply.

Note: The audio signal at U504-pin 46 should be approximately 12mV for 1.5kHz or 3kHz of deviation with 12.5kHz or 25kHz channel spacing.

The external microphone signal enters the radio on accessory connector P1 pin 2 and is routed via line EXT MIC to R5054. R5078 and R5076 provide the 9.3Vdc bias. Resistive divider R5054/ R5070 divide the input signal by 5.5 and provide input protection for the CMOS amplifier input. R5076 and C5009 provide a 510 ohm AC path to ground that sets the input impedance for the microphone and determines the gain based on the emitter resistor in the microphone's amplifier circuit.

C5047 serves as a DC blocking capacitor. The audio signal at U504-pin 48 should be approximately 14mV for 1.5kHz or 3kHz of deviation with 12.5kHz or 25kHz channel spacing.

The FLAT TX AUDIO signal from accessory connector P1-pin 5 is fed to the ASFIC CMP (U504 pin 42 through U509 pin 2 to U509 pin 15 via U506 OP-AMP circuit and C5057.

The ASFIC has an internal AGC that can control the gain in the mic audio path. The AGC can be disabled / enabled by the μ P. Another feature that can be enabled or disabled in the ASFIC is the VOX. This circuit, along with Capacitor C5023 at U504-pin 7, provides a DC voltage that can allow the μ P to detect microphone audio. The ASFIC can also be programmed to route the microphone audio to the speaker for public address operation.

7.2 PTT Sensing and TX Audio Processing

Internal microphone PTT is sensed by μ P U403 pin 71. Radio transmits when this pin is "0" and selects inside the ASFIC_CMP U504 internal Mic path. When the internal Mic PTT is "0" then external Mic PTT is grounded via D402. External Mic PTT is sensed by U403 pin 72 via Q412 circuits. The radio transmits when this pin is "0" and selects inside the ASFIC_CMP U504 External Mic path.

Inside the ASFIC CMP, the mic audio is filtered to eliminate frequency components outside the 300-3000Hz voice band, and pre-emphasized if pre-emphasis is enabled. The signal is then limited to prevent the transmitter from over deviating. The limited mic audio is then routed through a summer, which is used to add in signaling data, and then to a splatter filter to eliminate high frequency spectral components that could be generated by the limiter. The audio is then routed to an attenuator, which is tuned in the factory or the field to set the proper amount of FM deviation. The TX audio emerges from the ASFIC CMP at U504-pin 40 MOD IN, at which point it is routed to the RF section.

8.0 Transmit Signalling Circuits

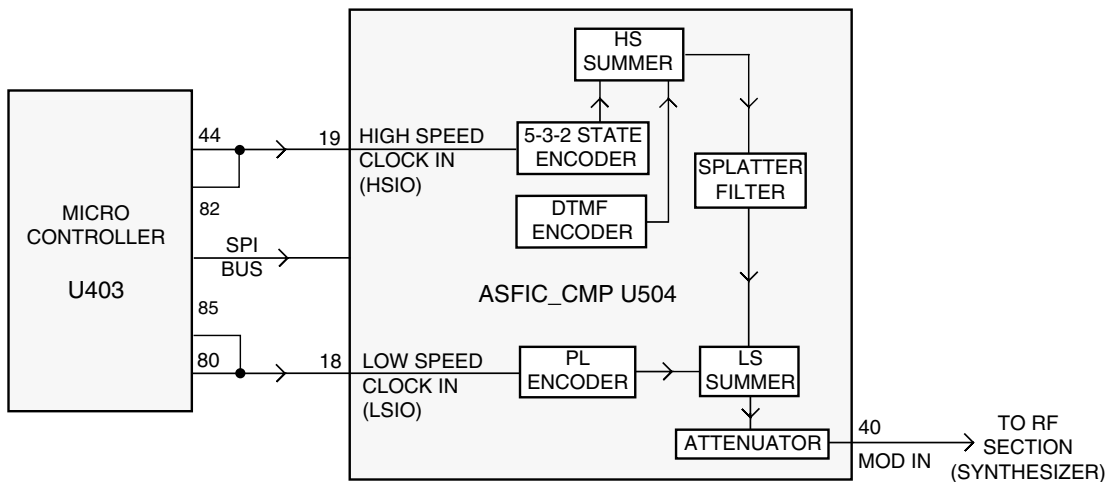


Figure 2-8 Transmit Signalling Path

From a hardware point of view, there are 3 types of signaling:

- Sub-audible data (PL / DPL / Connect Tone) that gets summed with transmit voice or signaling,
- DTMF data for telephone communication in trunked and conventional systems, and
- Audible signaling including MDC and high-speed trunking.

Note: All three types are supported by the hardware while the radio software determines which signaling type is available.

8.1 Sub-Audio Data (PL/DPL)

Sub-audible data implies signaling whose bandwidth is below 300Hz. PL and DPL waveforms are used for conventional operation and connect tones for trunked voice channel operation. The trunking connect tone is simply a PL tone at a higher deviation level than PL in a conventional system. Although it is referred to as “sub-audible data”, the actual frequency spectrum of these waveforms may be as high as 250 Hz, which is audible to the human ear. However, the radio receiver filters out any audio below 300Hz, so these tones are never heard in the actual system.

Only one type of sub-audible data can be generated by U504 (ASFIC CMP) at any one time. The process is as follows, using the SPI BUS, the μ P programs the ASFIC CMP to set up the proper low-speed data deviation and select the PL or DPL filters. The μ P then generates a square wave which strobes the ASFIC PL / DPL encode input LSIO U504-pin 18 at twelve times the desired data rate. For example, for a PL frequency of 103Hz, the frequency of the square wave would be 1236Hz.

This drives a tone generator inside U504 which generates a staircase approximation to a PL sine wave or DPL data pattern. This internal waveform is then low-pass filtered and summed with voice or data. The resulting summed waveform then appears on U504-pin 40 (MOD IN), where it is sent to the RF board as previously described for transmit audio. A trunking connect tone would be generated in the same manner as a PL tone.

8.2 High Speed Data

High speed data refers to the 3600 baud data waveforms, known as Inbound Signaling Words (ISWs) used in a trunking system for high speed communication between the central controller and the radio. To generate an ISW, the μ P first programs the ASFIC CMP (U504) to the proper filter and gain settings. It then begins strobing U504-pin 19 (HSIO) with a pulse when the data is supposed to change states. U504's 5-3-2 State Encoder (which is in a 2-state mode) is then fed to the post-limiter summer block and then the splatter filter. From that point it is routed through the modulation attenuator and then out of the ASFIC CMP to the RF board. MDC is generated in much the same way as trunking ISW. However, in some cases these signals may also pass through a data pre-emphasis block in the ASFIC CMP. Also these signaling schemes are based on sending a combination of 1200 Hz and 1800 Hz tones only. Microphone audio is muted during high speed data signaling.

8.3 Dual Tone Multiple Frequency (DTMF) Data

DTMF data is a dual tone waveform used during phone interconnect operation. It is the same type of tones which are heard when using a "Touch Tone" telephone.

There are seven frequencies, with four in the low group (697, 770, 852, 941Hz) and three in the high group (1209, 1336, 1477Hz). The high-group tone is generated by the μ P (U403-46) strobing U504-19 at six times the tone frequency for tones less than 1440Hz or twice the frequency for tones greater than 1440Hz. The low group tone is generated by the ASFIC CMP, controlled by the μ P via SPI bus. Inside U504 the low-group and high-group tones are summed (with the amplitude of the high group tone being approximately 2 dB greater than that of the low group tone) and then pre-emphasized before being routed to the summer and splatter filter. The DTMF waveform then follows the same path as was described for high-speed data.

9.0 Receive Audio Circuits

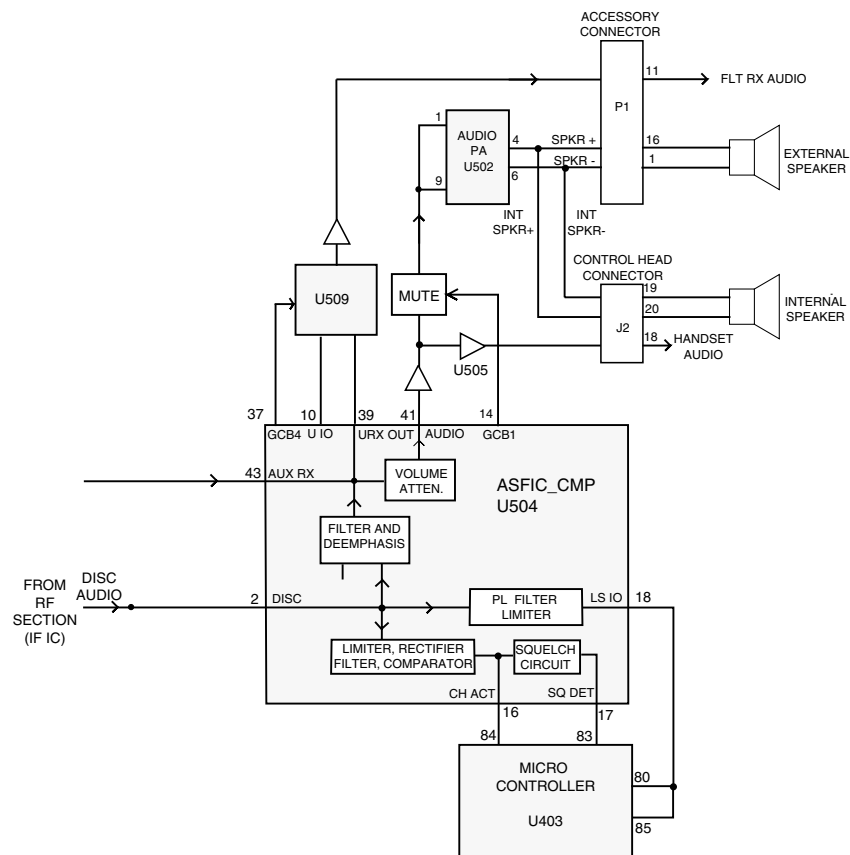


Figure 2-9 Receive Audio Paths

9.1 Squelch Detect

The radio's RF circuits are constantly producing an output at the discriminator (IF IC). This signal (DISC AUDIO) is routed to the ASFIC CMP's squelch detect circuitry input DISC (U504-pin 2). All of the squelch detect circuitry is contained within the ASFIC CMP. Therefore from a user's point of view, DISC AUDIO enters the ASFIC CMP, and the ASFIC CMP produces two CMOS logic outputs based on the result. They are CH ACT (U504-16) and SQ DET (U504-17).

The squelch signal entering the ASFIC CMP is amplified, filtered, attenuated, and rectified. It is then sent to a comparator to produce an active high signal on CH ACT. A squelch tail circuit is used to produce SQ DET (U504-17) from CH ACT. The state of CH ACT and SQ DET is high (logic "1") when carrier is detected, otherwise low (logic "0").

CH ACT is routed to the μ P pin 84 while SQ DET is routed to the μ P pin 83.

SQ DET is used to determine all audio mute / unmute decisions except for Conventional Scan. In this case CH ACT is a pre-indicator as it occurs slightly faster than SQ DET.

9.2 Audio Processing and Digital Volume Control

The receiver audio signal (DISC AUDIO) enters the controller section from the IF IC where it is DC coupled to ASFIC CMP via the DISC input U504-pin 2. The signal is then applied to both the audio and the PL/DPL paths

The audio path has a programmable amplifier, whose setting is based on the channel bandwidth being received, an LPF filter to remove any frequency components above 3000Hz, and a HPF to strip off any sub-audible data below 300Hz. Next, the recovered audio passes through a de-emphasis filter (if it is enabled to compensate for Pre-emphasis which is used to reduce the effects of FM noise). The IC then passes the audio through the 8-bit programmable attenuator whose level is set depending on the value of the volume control. Finally the filtered audio signal passes through an output buffer within the ASFIC CMP. The audio signal exits the ASFIC CMP at AUDIO output (U504 pin 41).

The μ P programs the attenuator, using the SPI BUS, based on the volume setting. The minimum / maximum settings of the attenuator are set by codeplug parameters.

Since sub-audible signaling is summed with voice information on transmit, it must be separated from the voice information before processing. Any sub-audible signaling enters the ASFIC CMP from the IF IC at DISC U504-2. Once inside, it goes through the PL/DPL path. The signal first passes through one of the two low-pass filters, either the PL low-pass filter or the DPL/LST low-pass filter. Either signal is then filtered and goes through a limiter and exits the ASFIC CMP at LSIO (U504-pin 18). At this point, the signal will appear as a square wave version of the sub-audible signal which the radio received. The μ P U403 pin 80 will decode the signal directly to determine if it is the tone / code which is currently active on that mode.

9.3 Audio Amplification Speaker (+) Speaker (-)

The output of the ASFIC CMP's digital volume pot, U504-pin 41 is routed through DC blocking capacitor C5049 to the audio PA (U502 pin 1 and 9).

The audio power amplifier has one inverted and one non-inverted output that produces the differential audio output SPK+/SPK- (U502 pins 4 and 6)

The audio PA is enabled via the ASFIC CMP (U504-GCB1). When the base of Q501 is low, the transistor is off and U502-pin 8 is high, using pull up resistor R5041, and the audio PA is ON. The voltage at U502-pin 8 must be above 8.5Vdc to properly enable the device.

If the voltage is between 3.3 and 6.4V, the device will be active but has its input (U502-pins 1/9) off. This is a mute condition which is used to prevent an audio pop when the PA is enabled.

The SPK+ and SPK- outputs of the audio PA have a DC bias which varies proportionately with B+ (U502- pin 7). B+ of 11V yields a DC offset of 5V, and B+ of 17V yields a DC offset of 8.5V. If either of these lines is shorted to ground, it is possible that the audio PA will be damaged. SPK+ and SPK- are routed to the accessory connector (P1-pin 1 and 16) and to the control head (connector J2-pins 19 and 20).

9.4 Handset Audio

Certain handheld accessories have a speaker within them which require a different voltage level than that provided by U502. For these devices HANDSET AUDIO is available at control head connector J2 pin18.

The received audio from the output of the ASFIC CMP's digital volume attenuator is routed to U505 pin 2 where it is amplified. This signal is routed from the output of the op-amp U505 to J2-pin 18. From the control head, the signal is sent directly to the microphone jack.

9.5 Filtered Audio and Flat Audio

The ASFIC CMP output audio at U504-pin 39 is filtered and de-emphasized, but has not gone through the digital volume attenuator. From ASFIC CMP U504-pin 39 the signal is routed via R5034 through gate U509-pin 12 and AC coupled to U505-pin 6. The gate controlled by ASFIC CMP port GCB4 selects between the filtered audio signal from the ASFIC CMP pin 39 (URXOUT) or the unfiltered (flat) audio signal from the ASFIC CMP pin 10 (UIO). Resistors R5034 and R5021 determine the gain of op-amp UU505-pin 6 for the filtered audio while R5032 and R5021 determine the gain for the flat Audio. The output of U505-pin 7 is then routed to P1 pin 11 via DC blocking capacitor C5003. Note that any volume adjustment of the signal on this path must be done by the accessory.

10.0 Receive Signalling Circuits

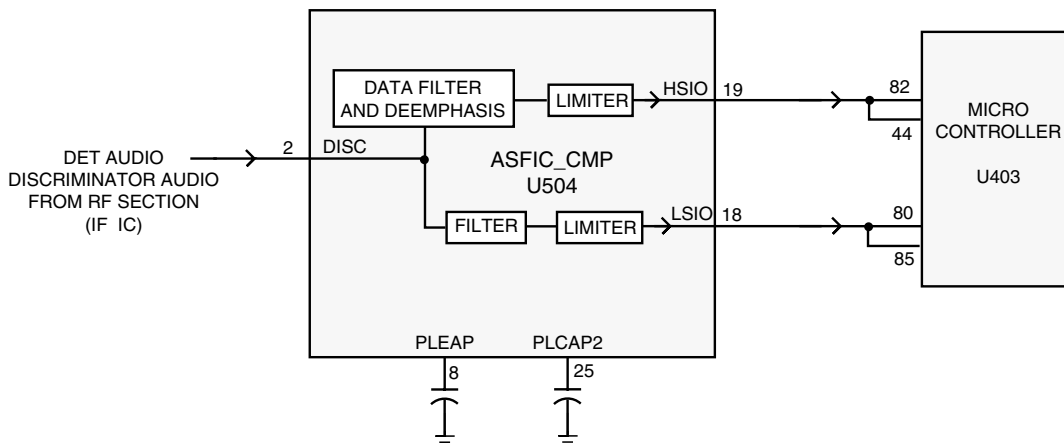


Figure 2-10 Receive Signalling Paths

10.1 Sub-Audio Data (PL/DPL) and High Speed Data Decoder

The ASFIC CMP (U504) is used to filter and limit all received data. The data enters the ASFIC CMP at input DISC (U504 pin 2). Inside U504 the data is filtered according to data type (HS or LS), then it is limited to a 0-3.3V digital level. The MDC and trunking high speed data appear at U504-pin 19, where it connects to the µP U403 pin 80.

The low speed limited data output (PL, DPL, and trunking LS) appears at U504-pin18, where it connects to the μ P U403-pin 80.

The low speed data is read by the μ P at twice the frequency of the sampling waveform; a latch configuration in the ASFIC CMP stores one bit every clock cycle. The external capacitors C5028, and C5026 set the low frequency pole for a zero crossings detector in the limiters for PL and HS data. The hysteresis of these limiters is programmed based on the type of received data.

10.2 Alert Tone Circuits

When the software determines that it needs to give the operator an audible feedback (for a good key press, or for a bad key press), or radio status (trunked system busy, phone call, circuit failures), it sends an alert tone to the speaker. It does so by sending SPI BUS data to U504 which sets up the audio path to the speaker for alert tones. The alert tone itself can be generated in one of two ways: internally by the ASFIC CMP, or externally using the μ P and the ASFIC CMP.

The allowable internal alert tones are 304, 608, 911, and 1823Hz. In this case a code contained within the SPI BUS load to the ASFIC CMP sets up the path and determines the tone frequency, and at what volume level to generate the tone. (It does not have to be related to the voice volume setting.)

For external alert tones, the μ P can generate any tone within the 100-3000Hz audio band. This is accomplished by the μ P generating a square wave which enters the ASFIC CMP at U504 pin 19. Inside the ASFIC CMP this signal is routed to the alert tone generator.

The output of the generator is summed into the audio chain just after the RX audio de-emphasis block. Inside U504, the tone is amplified and filtered, then passed through the 8-bit digital volume attenuator, which is typically loaded with a special value for alert tone audio. The tone exits at U504-pin 41 and is routed to the audio PA like receive audio.

Chapter 3

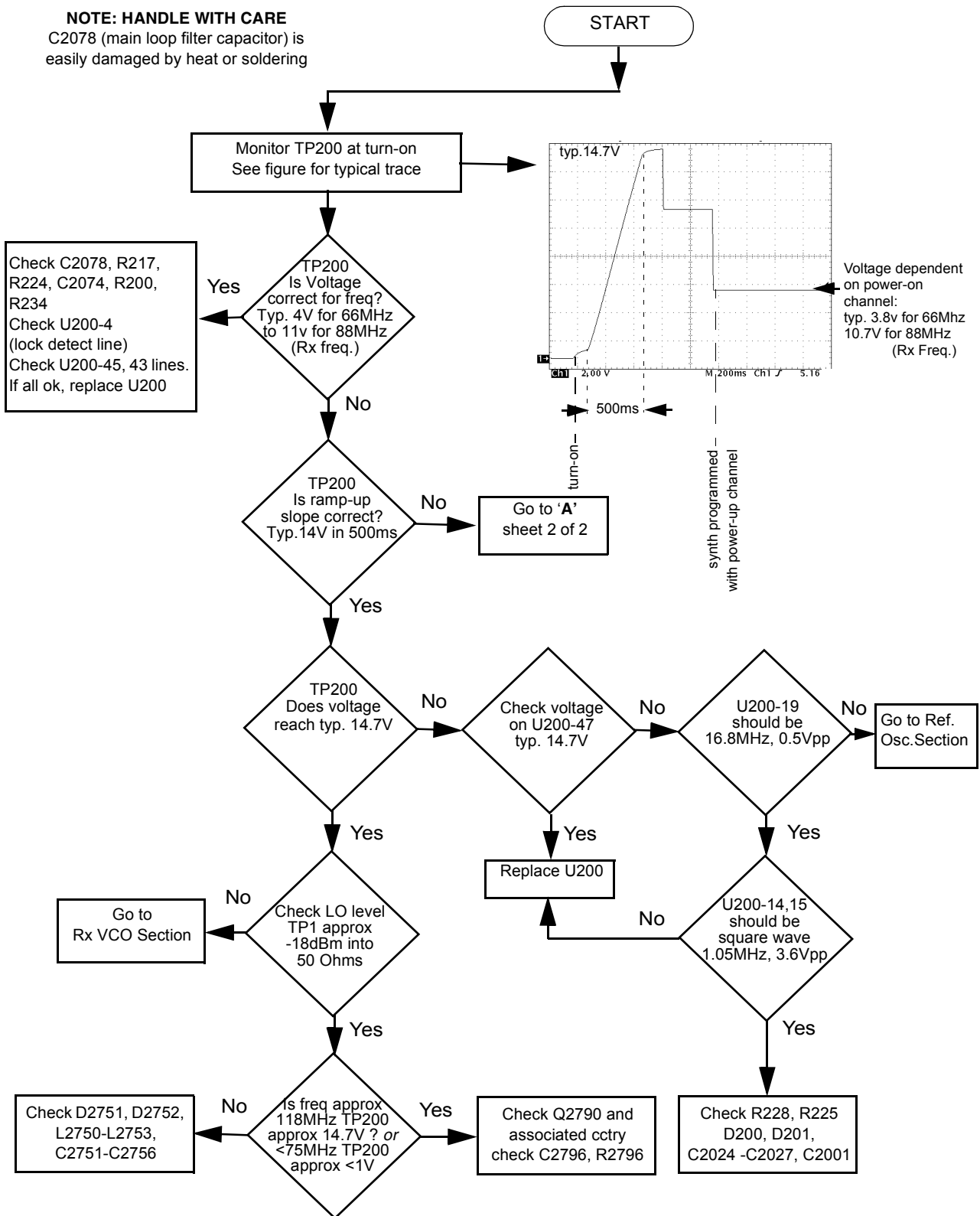
TROUBLESHOOTING CHARTS

This section contains detailed troubleshooting flowcharts. These charts should be used as a guide in determining the problem areas. They are not a substitute for knowledge of circuit operation and astute troubleshooting techniques. It is advisable to refer to the related detailed circuit descriptions in the theory of operation sections prior to troubleshooting a radio.

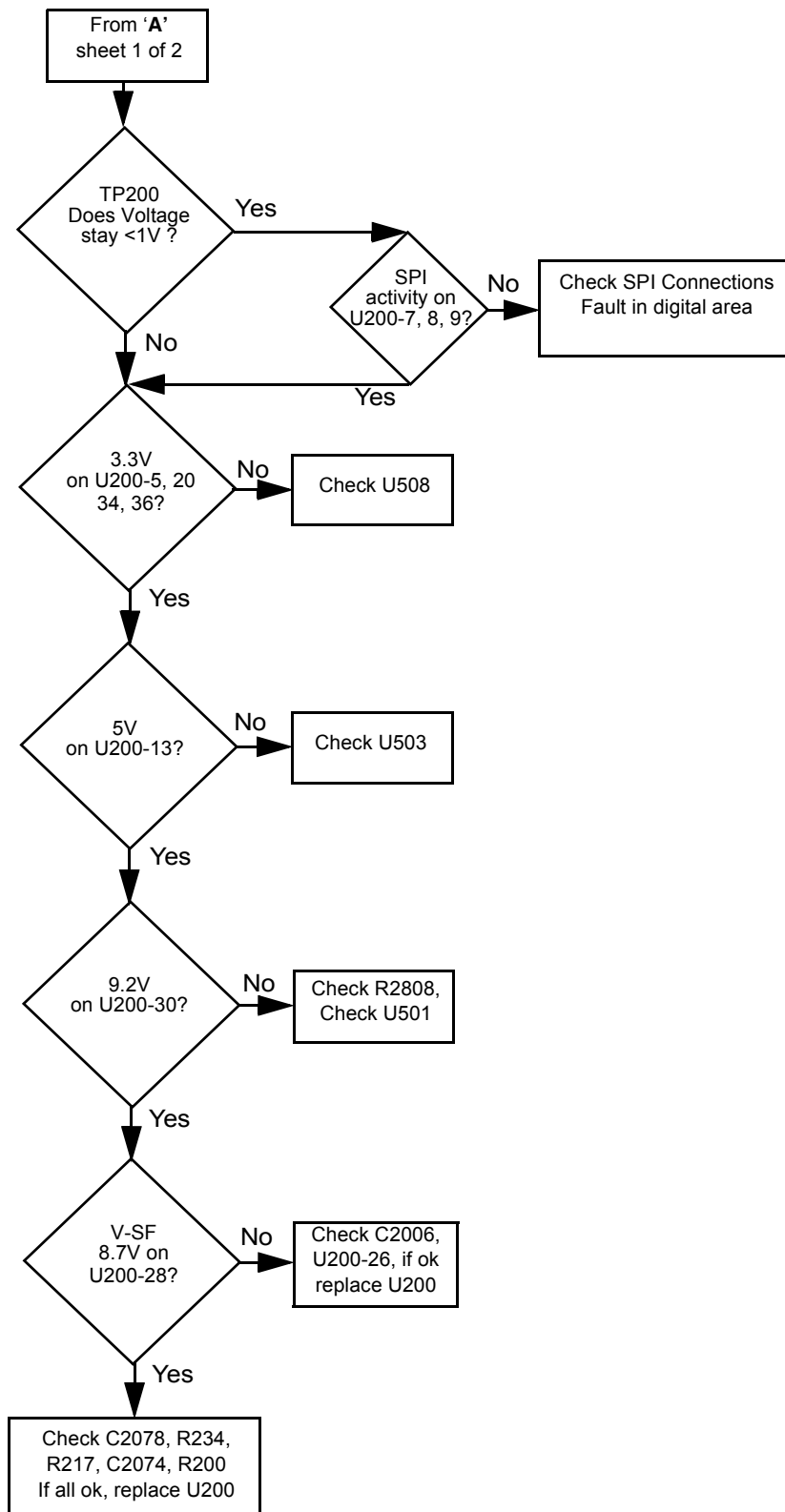
Most troubleshooting charts end up by pointing to an IC to replace. It is not always noted, but it is good practice to verify supplies and grounds to the affected IC and to trace continuity to the malfunctioning signal and related circuitry before replacing any IC. For instance, if a clock signal is not available at a destination, continuity from the source IC should be checked before replacing the source IC.

1.0 Troubleshooting Flow Chart for Out-of-Lock Receiver (Sheet 1 of 2)

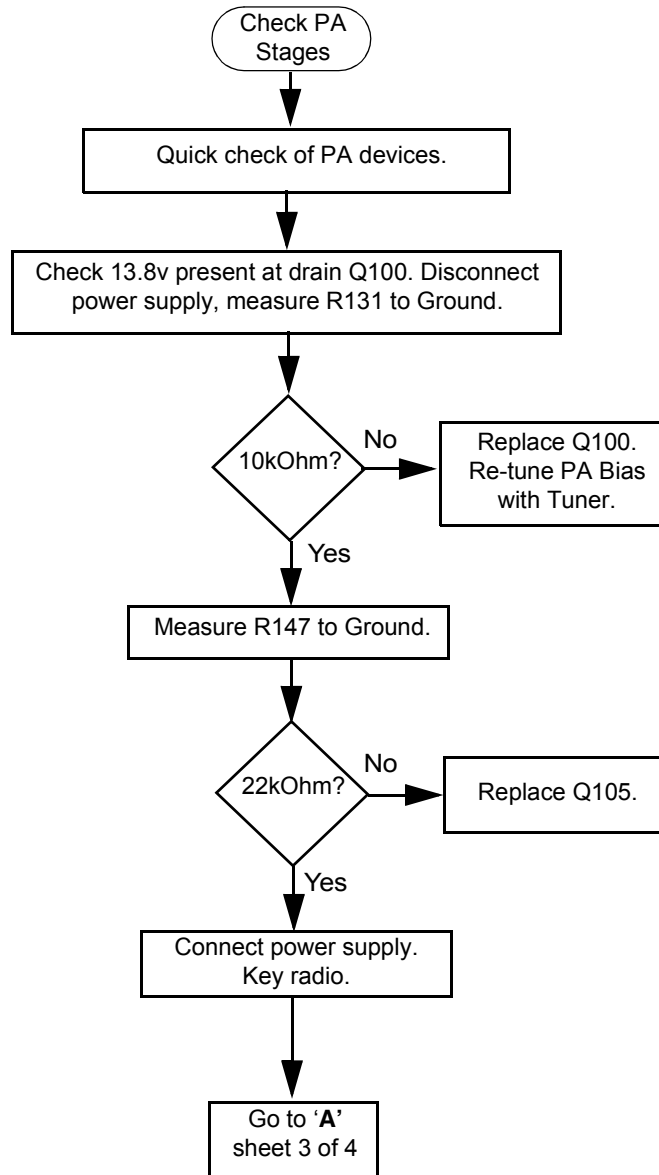
NOTE: HANDLE WITH CARE
 C2078 (main loop filter capacitor) is easily damaged by heat or soldering



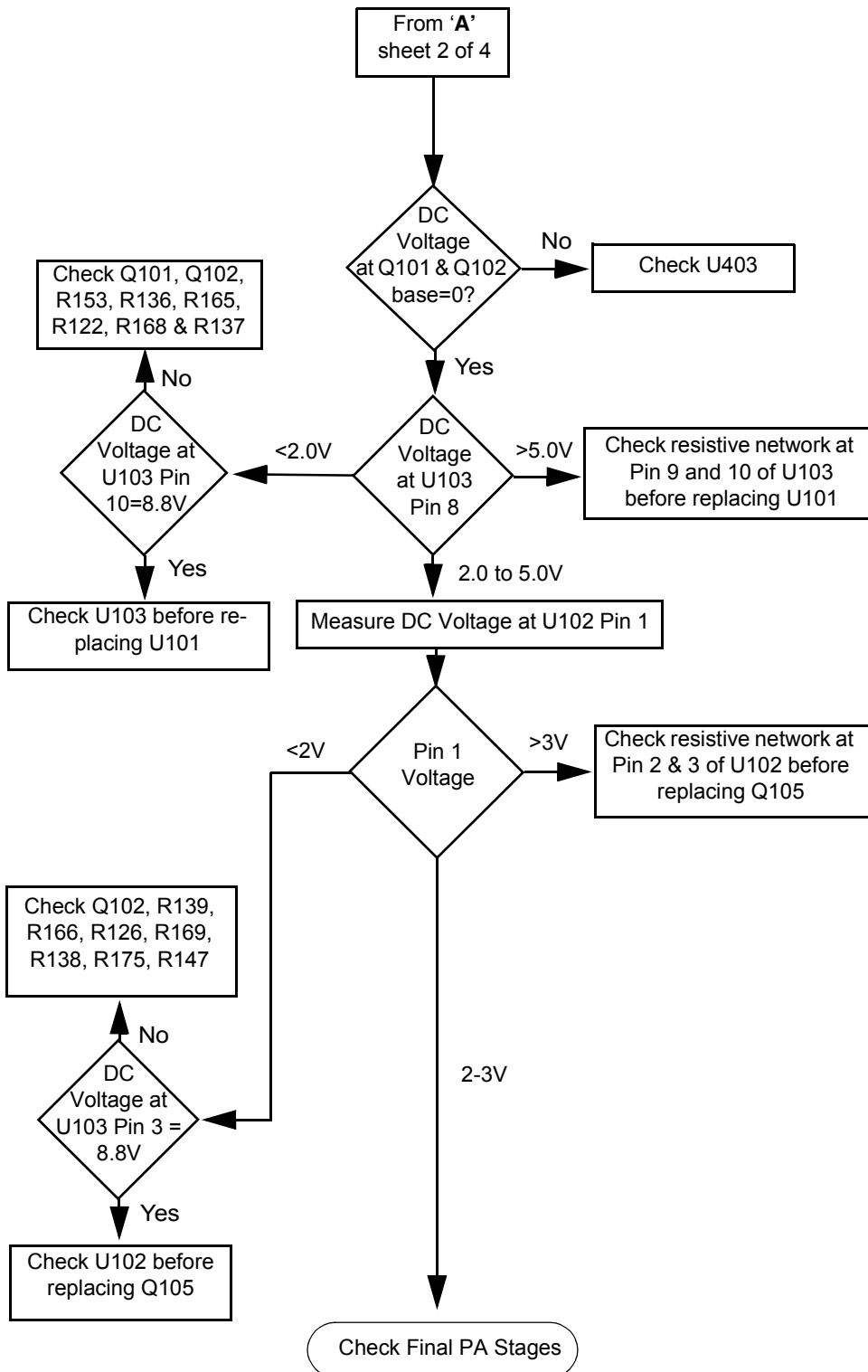
1.1 Troubleshooting Flow Chart for Out-of-Lock Receiver (Sheet 2 of 2)



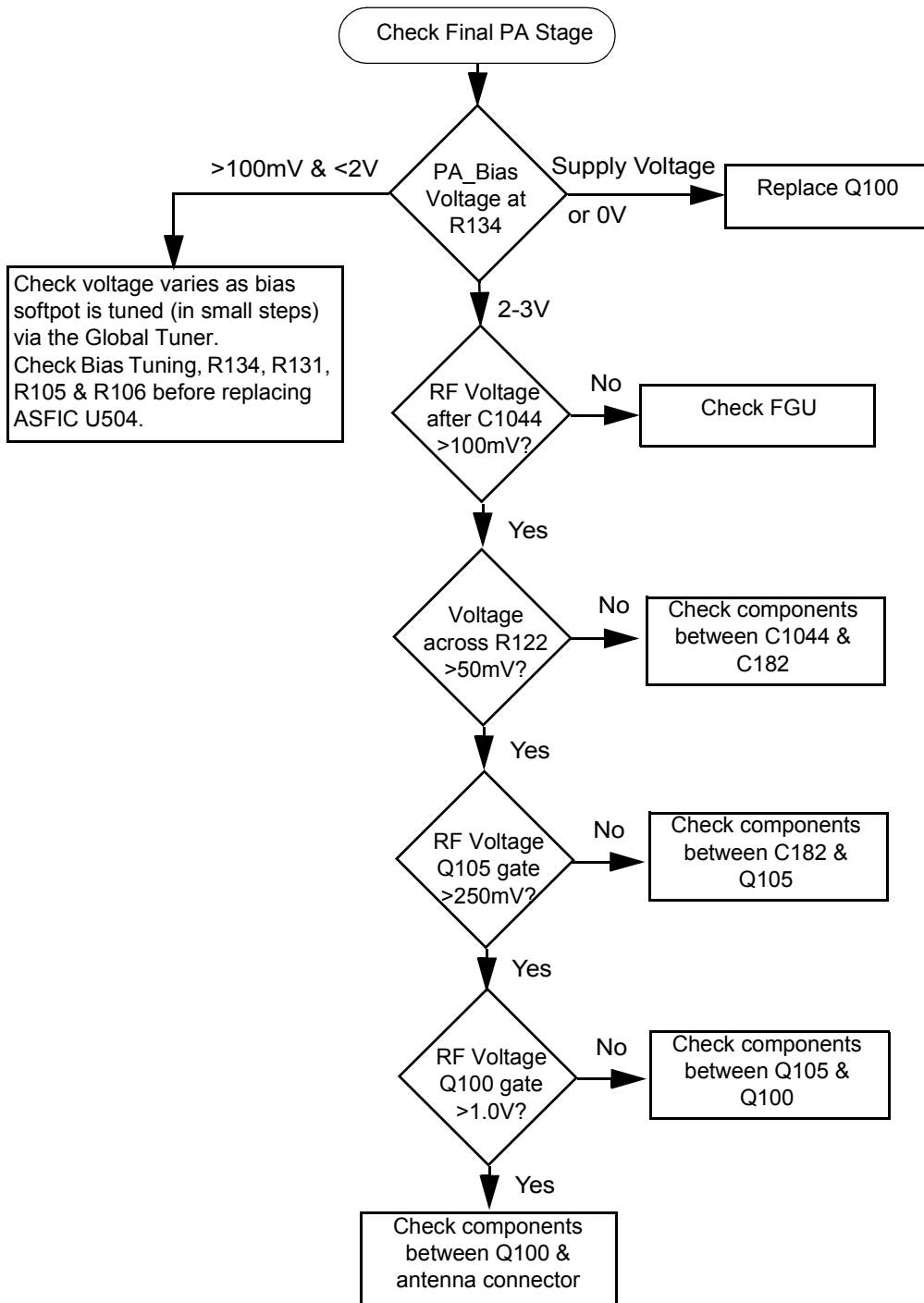
2.1 Troubleshooting Flow Chart for 25W Transmitter (Sheet 2 of 4)



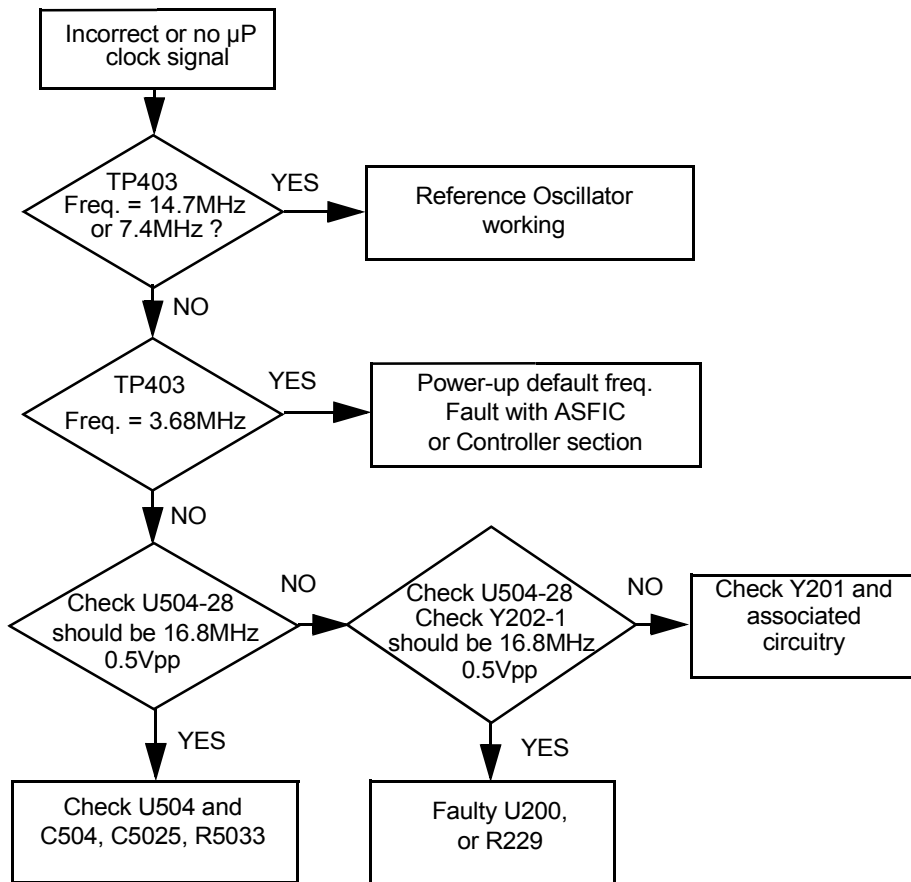
2.2 Troubleshooting Flow Chart for 25W Transmitter (Sheet 3 of 4)



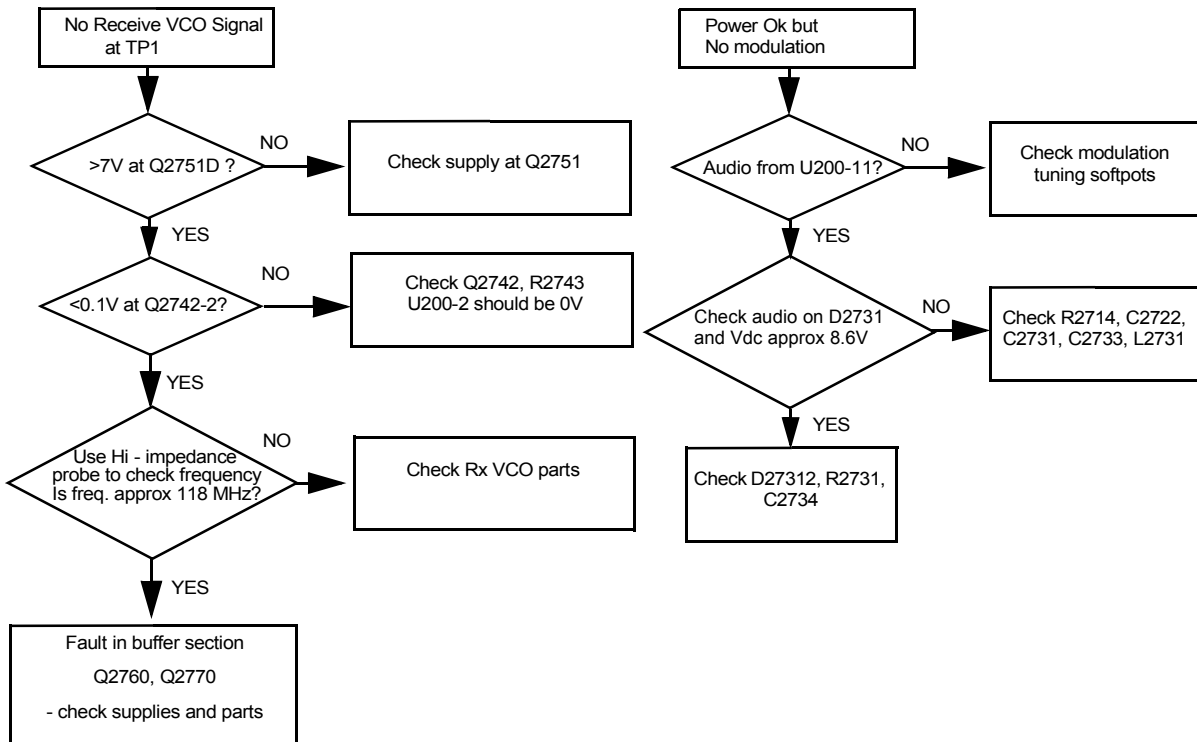
2.3 Troubleshooting Flow Chart for 25W Transmitter (Sheet 4 of 4)



3.0 Troubleshooting Flow Chart for Synthesizer (Reference Oscillator)



4.0 Troubleshooting Flow Chart for VCO



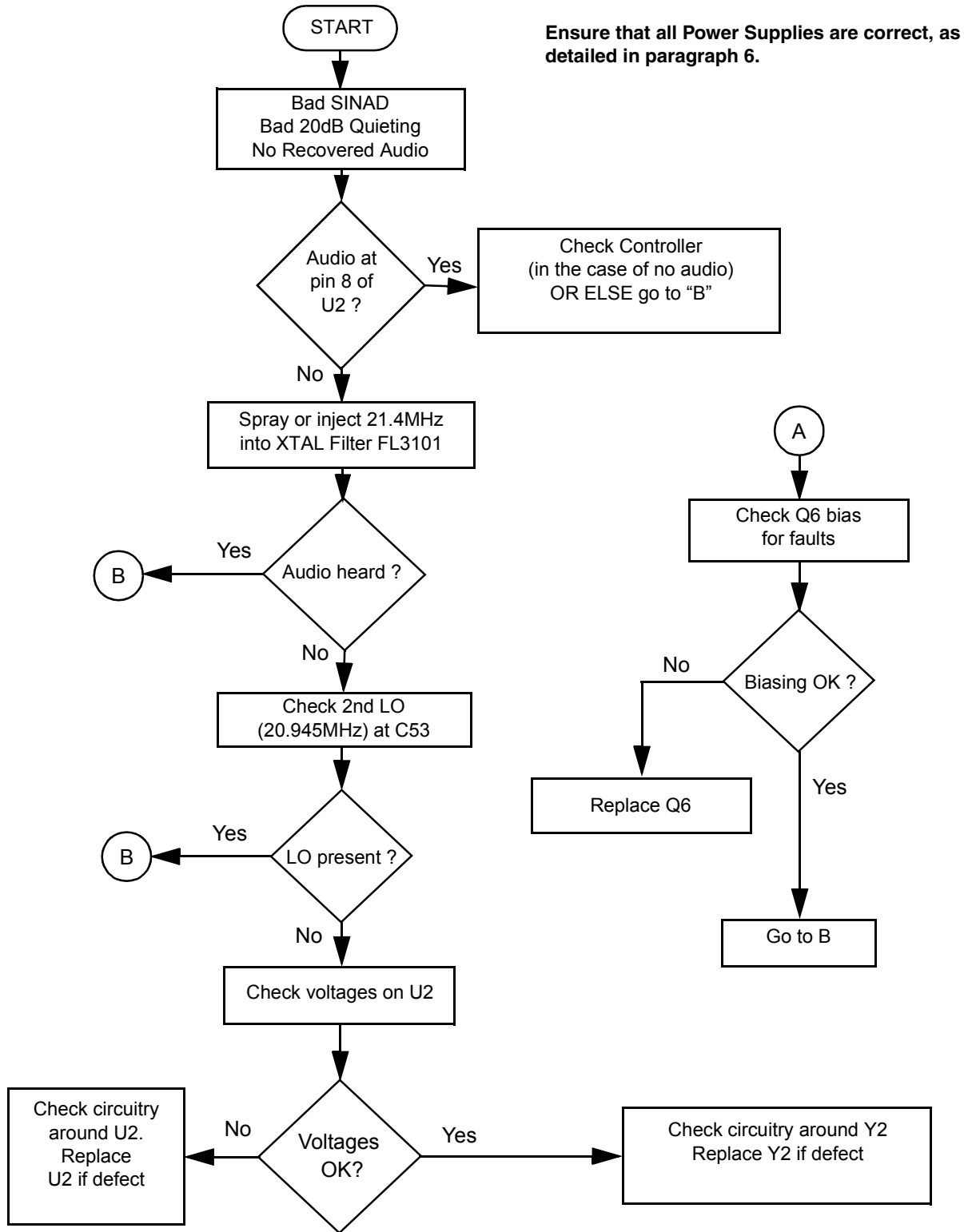
Out-of-Lock in TX

On detection of an out-of-lock in Tx, the radio returns to the Rx mode.

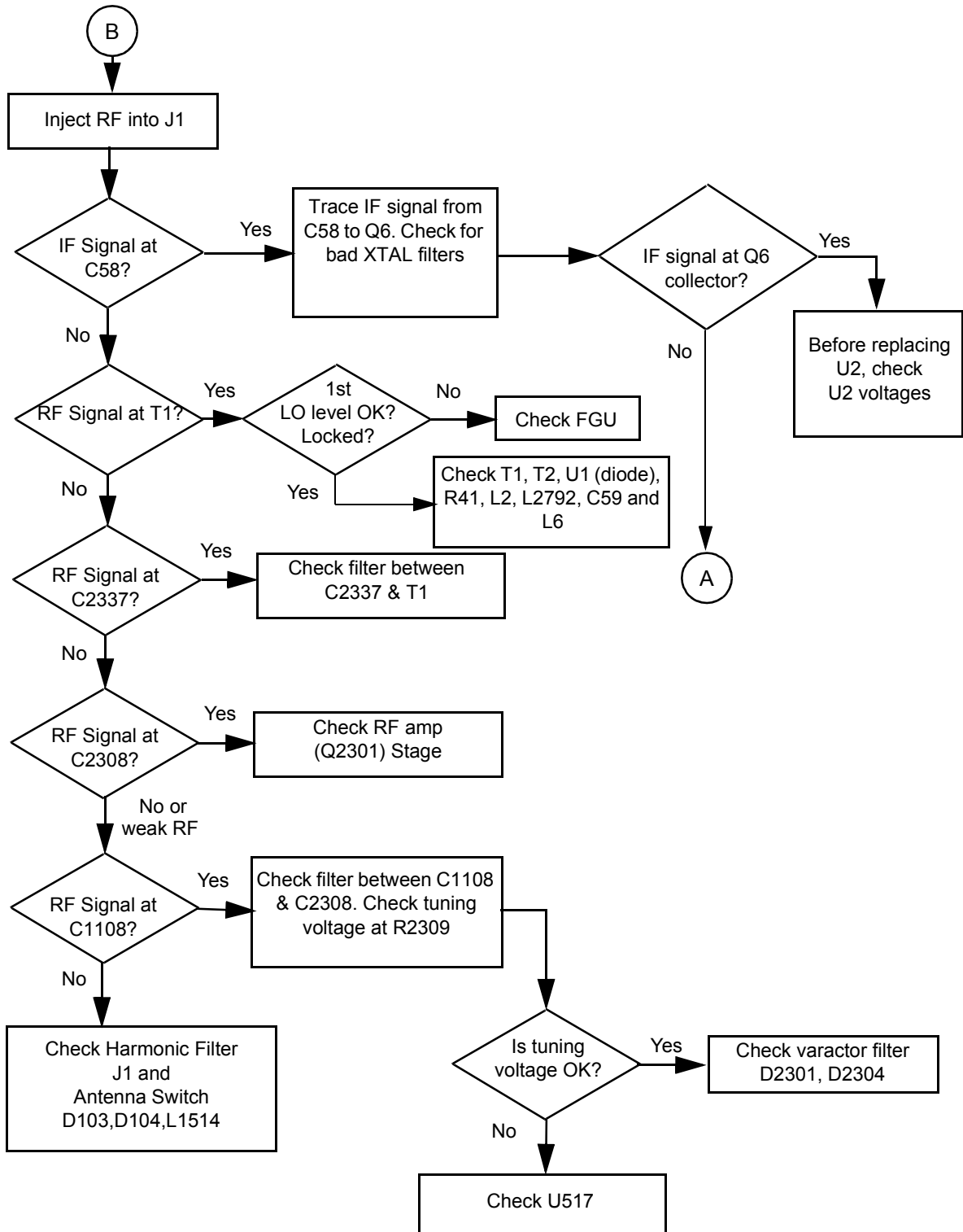
Check Rx - Tx switching
Q2742, Q2752 (should be turned on)
Check Q2741 and associated circuitry.

NOTE:
The TX VCO can be force enabled by grounding Q2742-3

5.0 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)

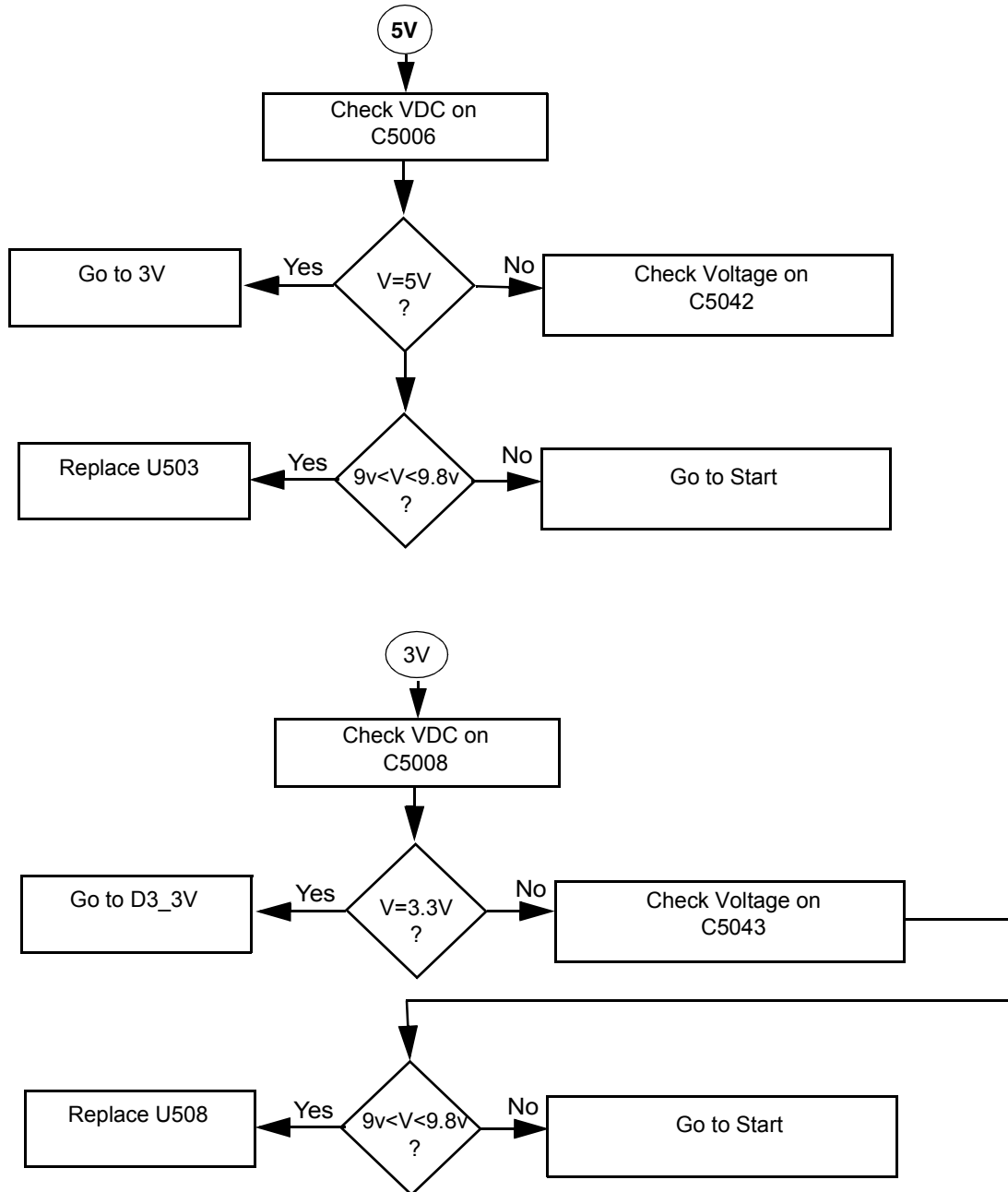


5.1 Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)

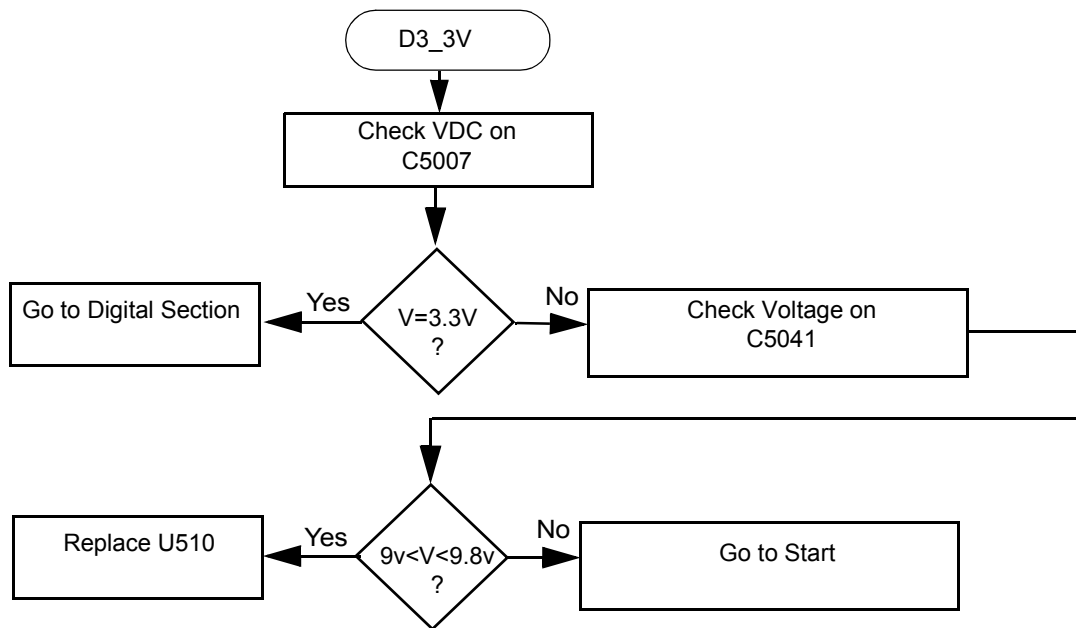


6.0 Troubleshooting Flow Chart for DC Supply (1 of 2)

Since the failure of a critical voltage supply might cause the radio to automatically power down, supply voltages should first be probed with a multimeter. If all the board voltages are absent, then the voltage test point should be retested using a rising-edge-triggered oscilloscope. If the voltage is still absent, then another voltage should be tested using the oscilloscope. If that voltage is present, then the original voltage supply in question is defective and requires investigation of associated circuitry.



6.1 Troubleshooting Flow Chart for DC Supply (2 of 2)



MIDBAND PCB/SCHEMATICS/PARTS LISTS

1.0 Allocation of Schematics and Circuit Boards

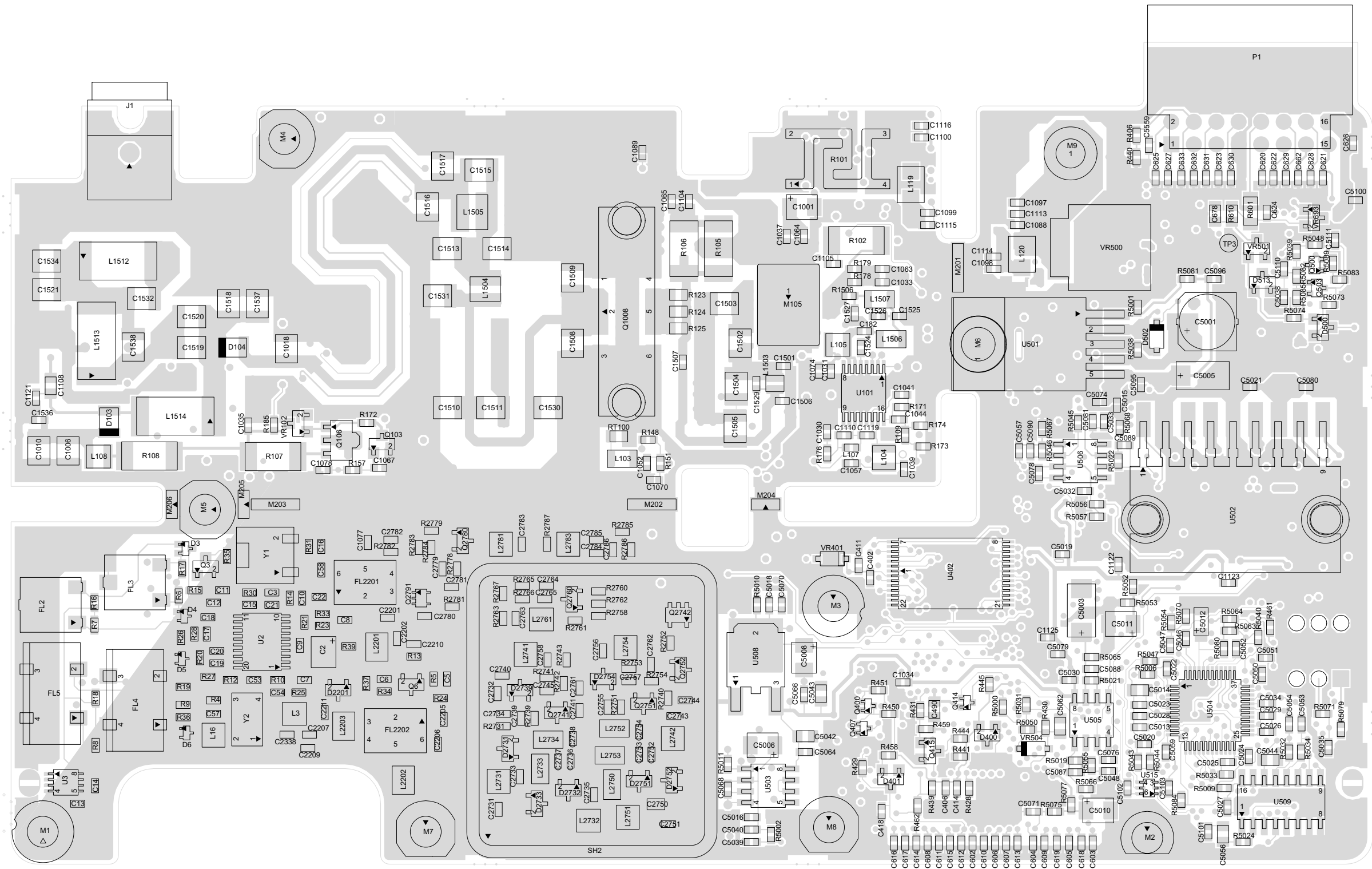
1.1 Midband and Controller Circuits

The Midband circuits are contained on the printed circuit board (PCB) which also contains the Controller circuits. This Chapter shows the schematics for both the Midband circuits and the Controller circuits. The PCB component layouts and the Parts Lists in this Chapter show both the Controller and Midband circuit components. The Midband and Controller schematics and the related PCB and parts list are shown in the tables below.

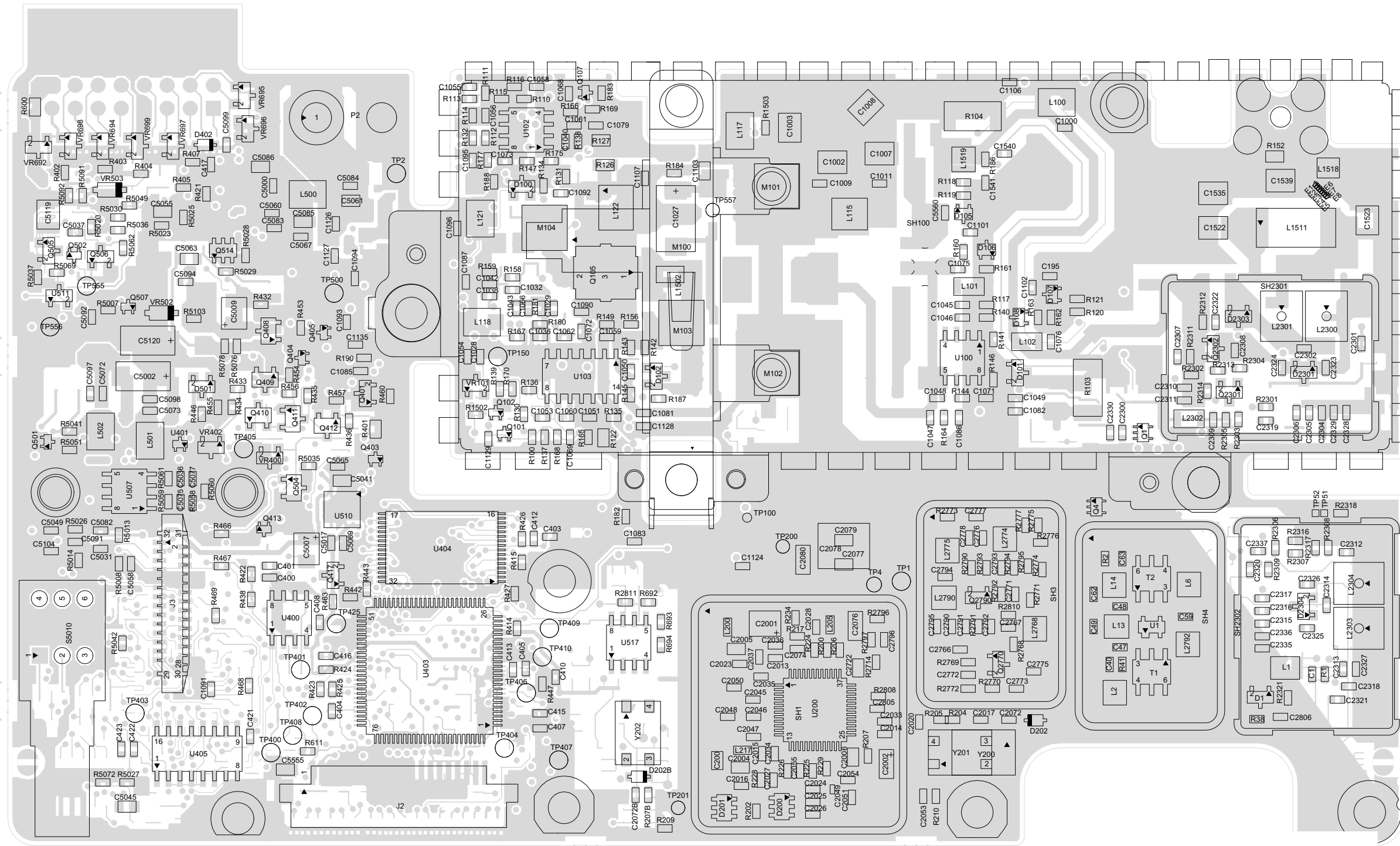
Table 4-1 Midband 1-25W Diagrams and Parts Lists

PCB : 8489012U01-C Main Board Top Side 8489012U01-C Main Board Bottom Side	Page 4-3 Page 4-4
SCHEMATICS Main Circuit Transmitter Synthesiser and VCO Receiver Front and Back End DC and Audio Ccts Microprocessor and Controller Ccts	Page 4-5 Page 4-6 Page 4-7 Page 4-8 Page 4-9 Page 4-10
Parts List 8489012U01-C	Page 4-11
Controller version is T1	

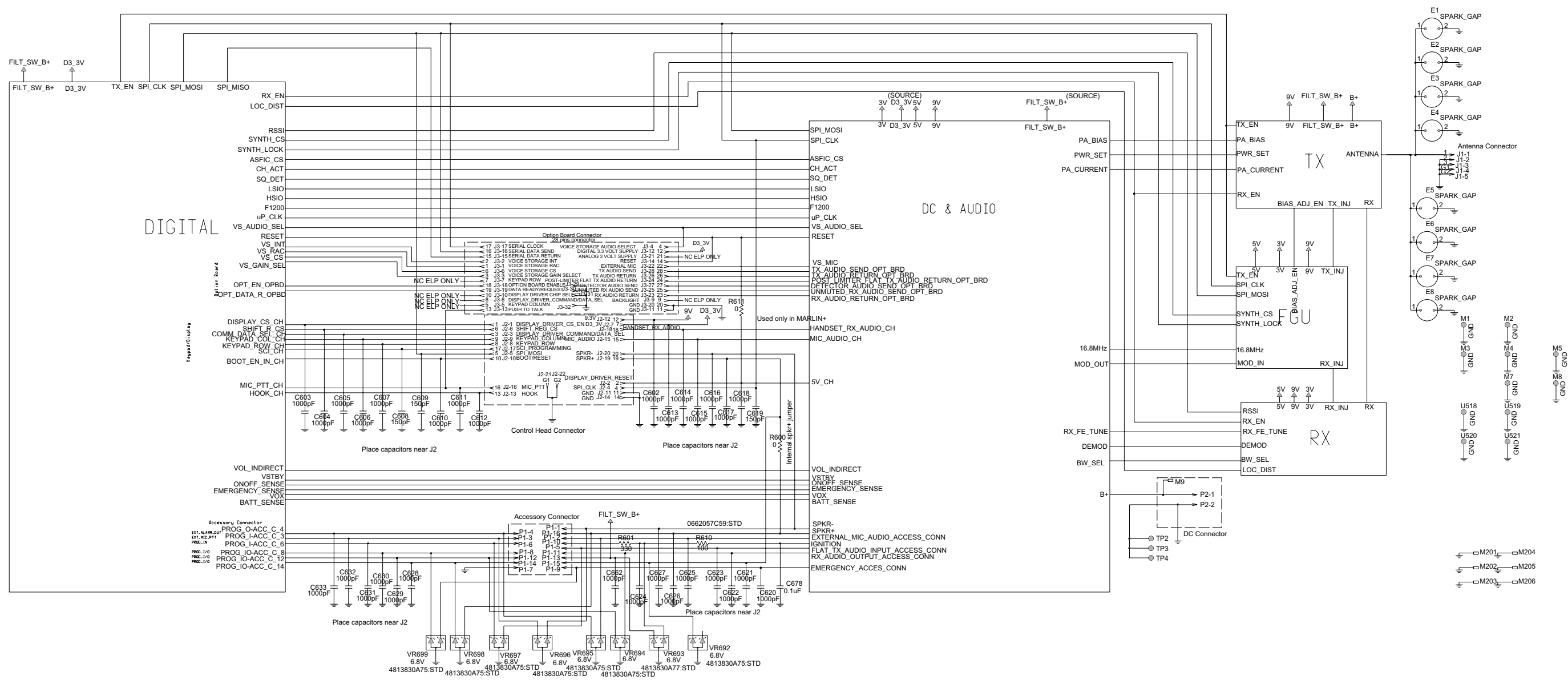
2.0 Midband 1-25W PCB 8489012U01 (rev. C) / Schematics



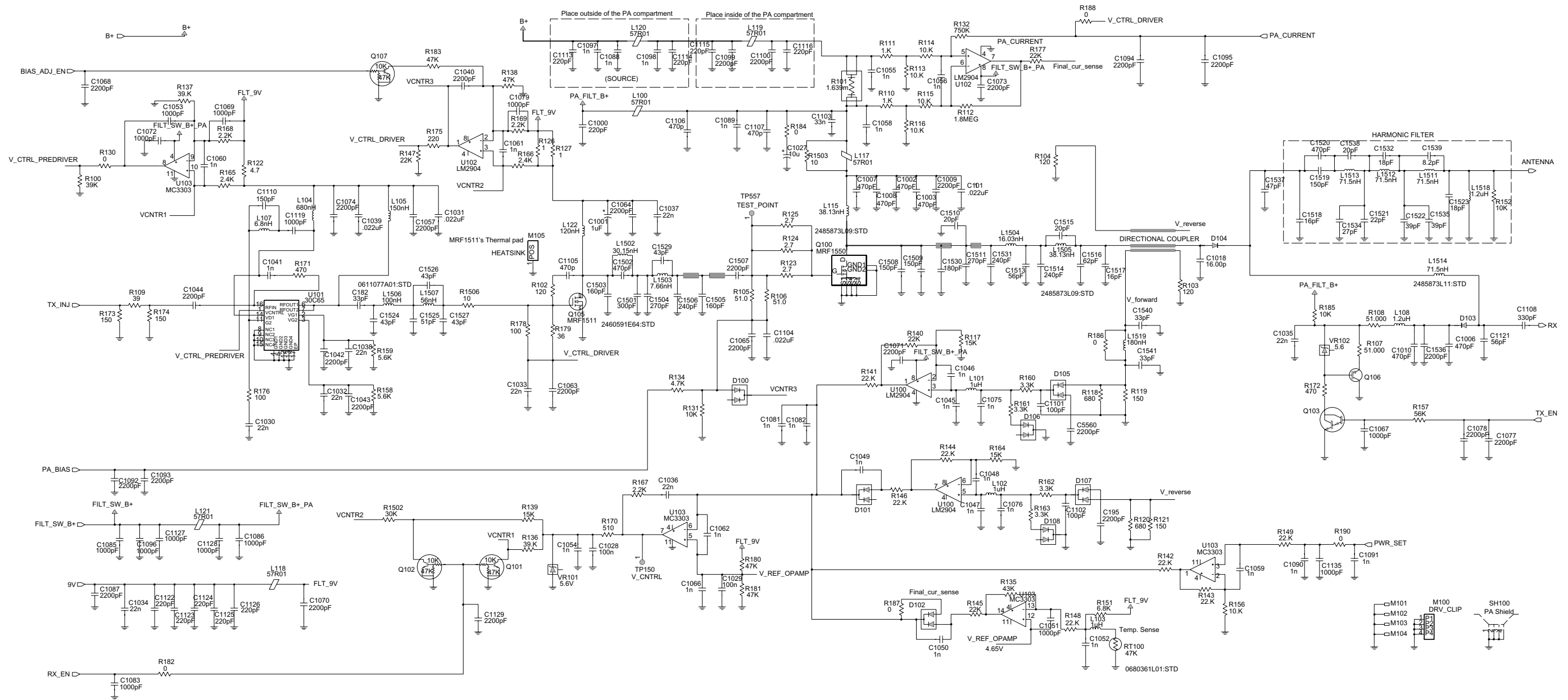
Midband (66-88MHz) 1-25W 8489012U01 (rev. C)



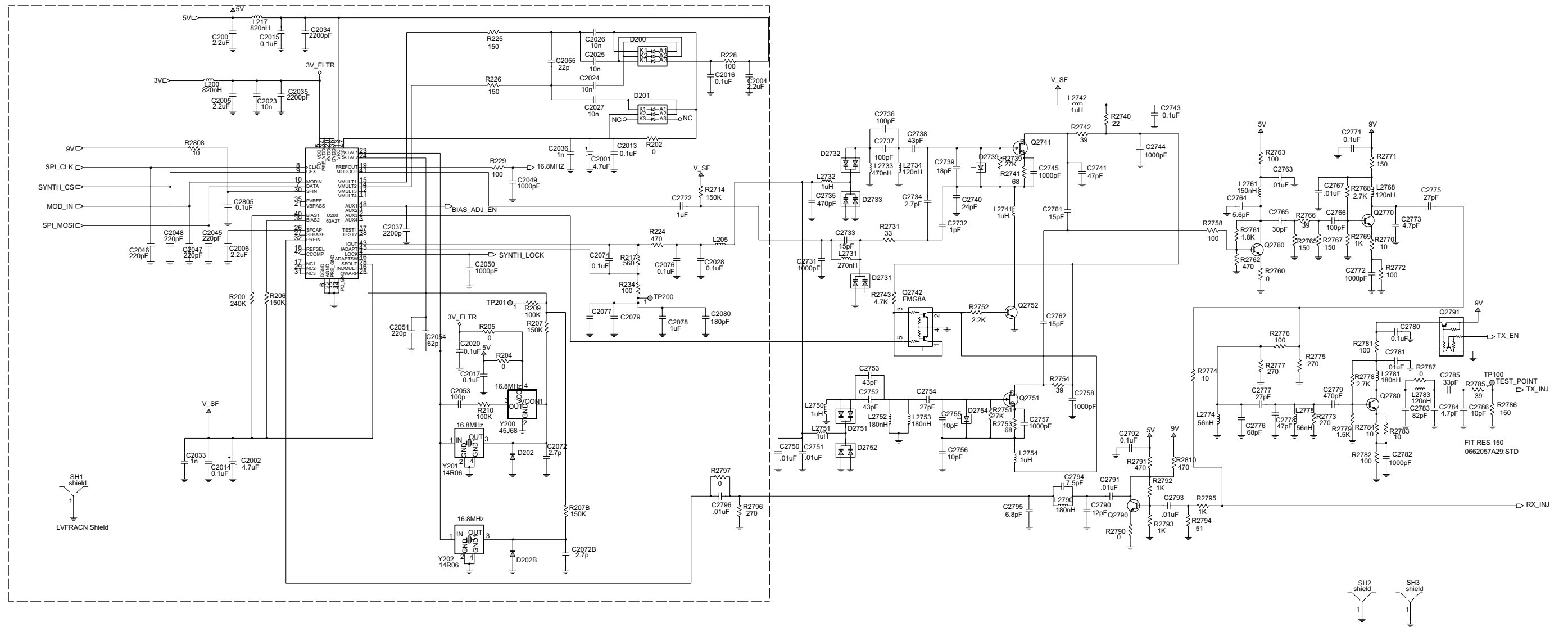
Midband (66-88MHz) 1-25W 8489012U01 (rev. C)



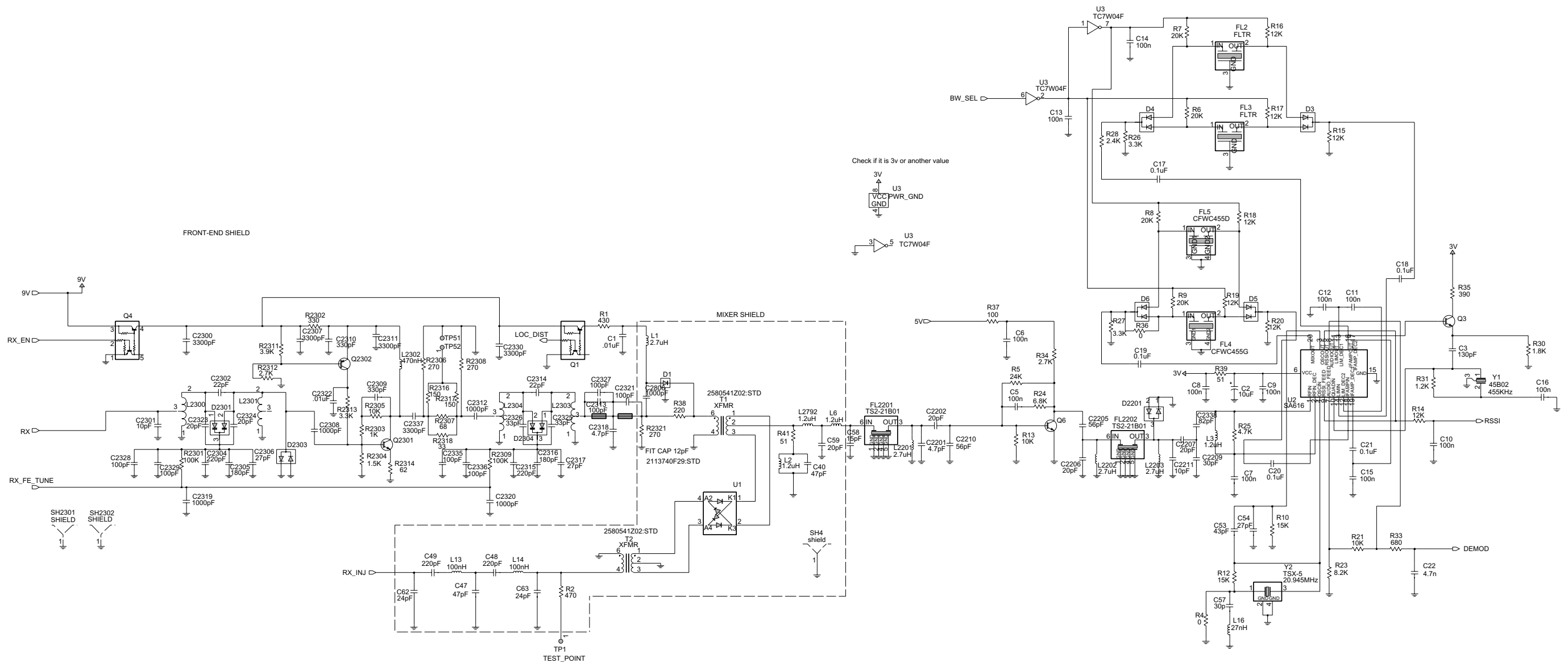
Midband (66-88MHz) Main Circuit



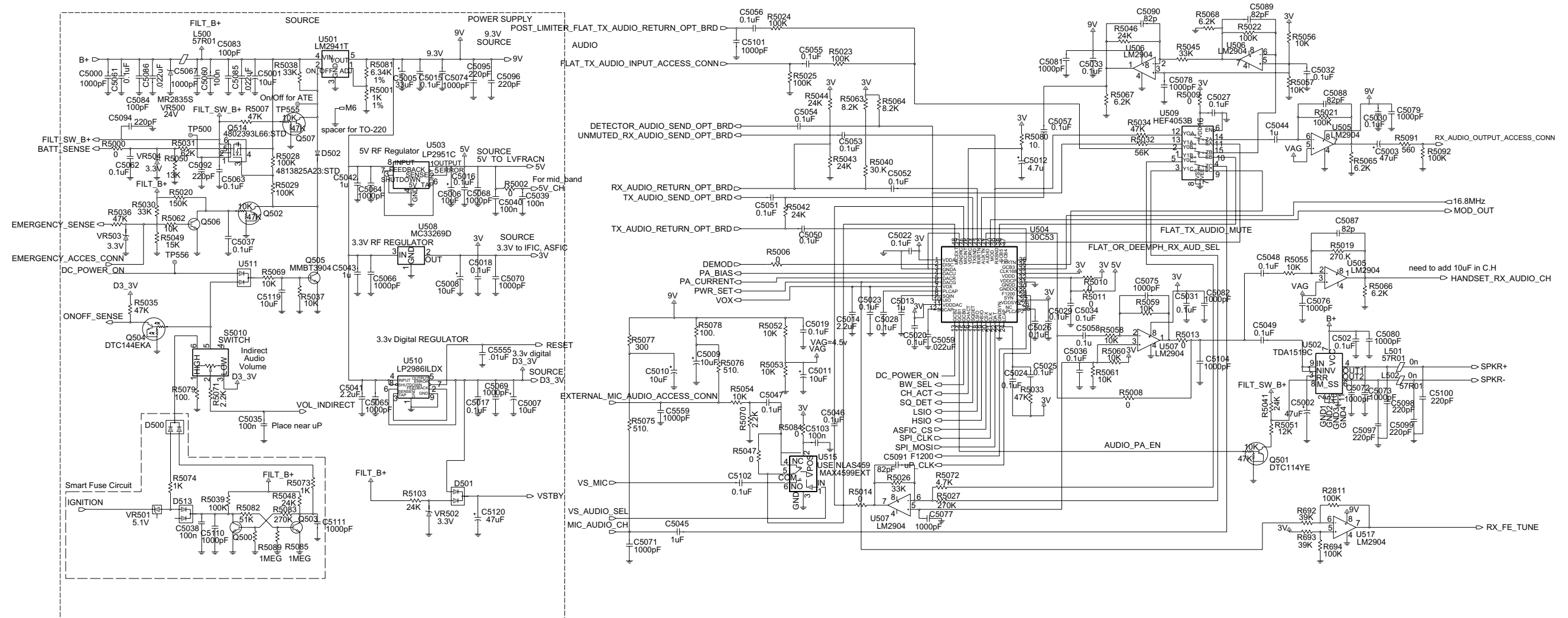
Midband (66-88MHz) Transmitter



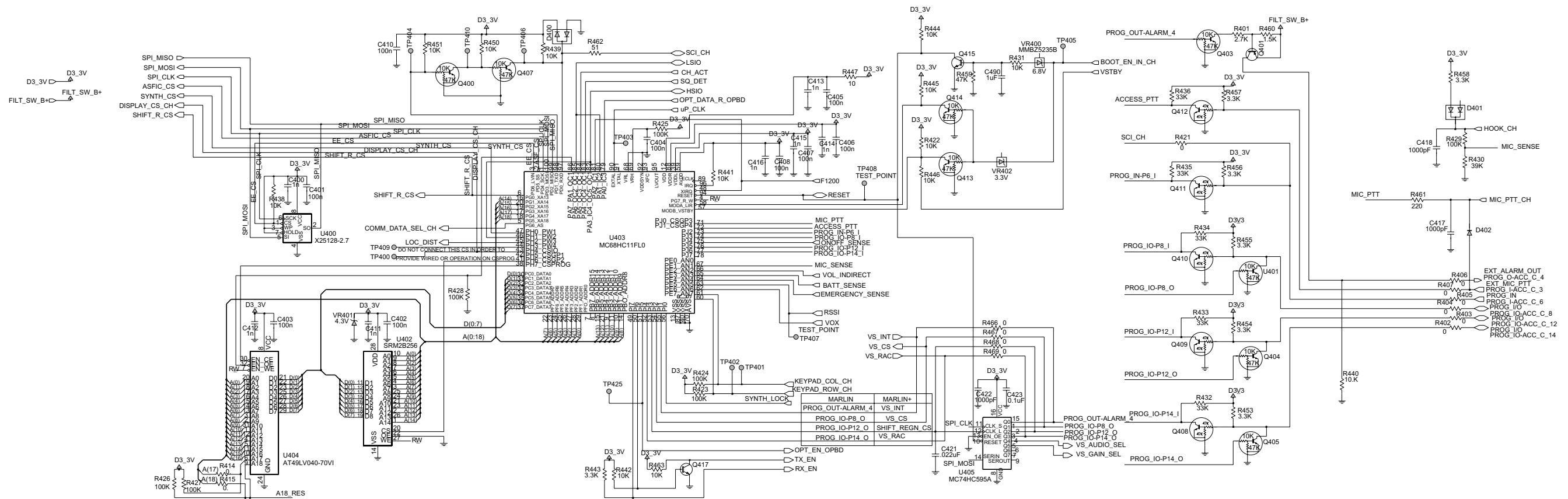
Midband (66-88MHz) Synthesiser and VCO



Midband (66-88MHz) Receiver



Midband (66-88MHz) DC and Audio Circuits



Midband (66-88MHz) Microprocessor and Controller

2.1 MB PCB 8489012U01 (rev. C) Parts List 1-25W

Circuit Ref.	Motorola Part No.	Description
C1	2113741F49	CAP .01uF
C2	2311049A57	CAPP 10uF
C3	2113740F54	CAP130pF
C5	2113743E20	CAP 100n
C6	2113743E20	CAP100n
C7	2113743E20	CAP100n
C8	2113743E20	CAP100n
C9	2113743E20	CAP100n
C10	2113743E20	CAP100n
C11	2113743E20	CAP100n
C12	2113743E20	CAP100n
C13	2113743E20	CAP100n
C14	2113743E20	CAP100n
C15	2113743E20	CAP100n
C16	2113743E20	CAP100n
C17	2113743E20	CAP 0.1uF
C18	2113743E20	CAP 0.1uF
C19	2113743E20	CAP 0.1uF
C20	2113743E20	CAP 0.1uF
C21	2113743E20	CAP 0.1uF
C22	2113741F41	CAP 4.7n
C40	2113740F43	CAP 47pF
C47	2113740F43	CAP 47pF
C48	2113740F59	CAP 220pF
C49	2113740F59	CAP 220pF
C53	2113740F42	CAP 43pF
C54	2113740F37	CAP 27pF
C57	NOT PLACED	CAP 30p
C58	2113740F31	CAP 15pF

Circuit Ref.	Motorola Part No.	Description
C59	2113740F34	CAP 20pF
C62	2113740F36	CAP 24pF
C63	2113740F36	CAP 24pF
C182	2113740F39	CAP 33pF
C195	2113741F33	CAP 2200pF
C200	2113743F18	CAP 2.2uF
C400	2113741F25	CAP1n
C401	2113743K15	CAP100n
C402	2113743K15	CAP100n
C403	2113743K15	CAP100n
C404	2113743K15	CAP100n
C405	2113743K15	CAP100n
C406	2113743K15	CAP100n
C407	2113743K15	CAP100n
C408	2113743K15	CAP100n
C410	2113743K15	CAP100n
C411	2113741F25	CAP1n
C412	2113741F25	CAP1n
C413	2113741F25	CAP1n
C414	2113741F25	CAP1n
C415	2113741F25	CAP1n
C416	2113741F25	CAP1n
C417	2113741F25	CAP1000pF
C418	2113741F25	CAP1000pF
C419	NOT PLACED	CAP.01uF
C421	2113743E07	CAP.022uF
C422	2113741F25	CAP1000pF
C423	2113743K15	CAP0.1uF
C490	NOT PLACED	CAP 1uF
C602	2113741F25	CAP1000pF

Circuit Ref.	Motorola Part No.	Description
C603	2113741F25	CAP1000pF
C604	2113741F25	CAP1000pF
C605	2113741F25	CAP1000pF
C606	2113741F25	CAP1000pF
C607	2113741F25	CAP1000pF
C608	NOT PLACED	CAP150pF
C609	NOT PLACED	CAP150pF
C610	2113741F25	CAP1000pF
C611	2113741F25	CAP1000pF
C612	2113741F25	CAP1000pF
C613	2113741F25	CAP1000pF
C614	2113741F25	CAP1000pF
C615	2113741F25	CAP1000pF
C616	2113741F25	CAP1000pF
C617	2113741F25	CAP1000pF
C618	2113741F25	CAP1000pF
C619	NOT PLACED	CAP150pF
C620	2113741F25	CAP1000pF
C621	2113741F25	CAP1000pF
C622	2113741F25	CAP1000pF
C623	2113741F25	CAP1000pF
C624	2113741F25	CAP1000pF
C625	2113741F25	CAP1000pF
C626	2113741F25	CAP1000pF
C627	2113741F25	CAP1000pF
C628	2113741F25	CAP1000pF
C629	2113741F25	CAP1000pF
C630	2113741F25	CAP1000pF
C631	2113741F25	CAP1000pF
C632	2113741F25	CAP1000pF

Circuit Ref.	Motorola Part No.	Description
C633	2113741F25	CAP1000pF
C662	2113741F25	CAP1000pF
C678	2113741M69	CAP 0.1uF
C1000	NOT PLACED	CAP220pF
C1001	2311049A08	CAP 1uF
C1002	2111078B59	CAP 470pF
C1003	2111078B59	CAP 470pF
C1006	2111078B59	CAP 470pF
C1007	2111078B59	CAP 470pF
C1008	2111078B59	CAP 470pF
C1009	NOT PLACED	CAP 2200pF
C1010	2111078B59	CAP470pF
C1011	NOT PLACED	CAP .022uF
C1018	NOT PLACED	CAP16.00p
C1027	NOT PLACED	CAP10u
C1028	2113743K15	CAP 100n
C1029	2113743K15	CAP100n
C1030	2113743E07	CAP 22n
C1031	2113743E07	CAP .022uF
C1032	2113743E07	CAP 22n
C1033	2113743E07	CAP 22n
C1034	2113743E07	CAP 22n
C1035	2113743E07	CAP 22n
C1036	2113743E07	CAP 22n
C1037	2113743E07	CAP 22n
C1038	2113743E07	CAP 22n
C1039	2113743E07	CAP .022uF
C1040	2113741F33	CAP 2200pF
C1041	2113741F25	CAP1n
C1042	2113741F33	CAP 2200pF

Circuit Ref.	Motorola Part No.	Description
C1043	2113741F33	CAP 2200pF
C1044	2113741F33	CAP 2200pF
C1045	2113741F25	CAP1n
C1046	2113741F25	CAP 1n
C1047	2113741F25	CAP 1n
C1048	2113741F25	CAP1n
C1049	2113741F25	CAP1n
C1050	2113741F25	CAP1n
C1051	2113741F25	CAP1000pF
C1052	2113741F25	CAP1n
C1053	2113741F25	CAP1000pF
C1054	2113741F25	CAP1n
C1055	2113741F25	CAP1n
C1056	2113741F25	CAP1n
C1057	2113741F33	CAP 2200pF
C1058	2113741F25	CAP1n
C1059	2113741F25	CAP1n
C1060	2113741F25	CAP1n
C1061	2113741F25	CAP1n
C1062	2113741F25	CAP1n
C1063	2113741F33	CAP 2200pF
C1064	2113741F33	CAP 2200pF
C1065	2113741F33	CAP 2200pF
C1066	2113741F25	CAP1n
C1067	2113741F25	CAP1000pF
C1068	NOT PLACED	CAP 2200pF
C1069	2380090M24	CAPP10uF
C1070	2113741F33	CAP 2200pF
C1071	2113741F33	CAP 2200pF
C1072	2113741F25	CAP1000pF

Circuit Ref.	Motorola Part No.	Description
C1073	2113741F33	CAP 2200pF
C1074	2113741F33	CAP 2200pF
C1075	2113741F25	CAP1n
C1076	2113741F25	CAP1n
C1077	2113741F33	CAP 2200pF
C1078	2113741F33	CAP 2200pF
C1081	2113741F25	CAP1n
C1082	2113741F25	CAP1n
C1083	NOT PLACED	CAP1000pF
C1084	NOT PLACED	CAP 2200pF
C1085	2113741F25	CAP 1000pF
C1086	2113741F25	CAP1000pF
C1087	NOT PLACED	CAP 2200pF
C1088	2113741F25	CAP1n
C1089	2113741F25	CAP1n
C1090	2113741F25	CAP1n
C1091	2113741F25	CAP1n
C1092	NOT PLACED	CAP 2200pF
C1093	NOT PLACED	CAP 2200pF
C1094	2113741F33	CAP 2200pF
C1095	2113741F33	CAP 2200pF
C1096	2113741F25	CAP1000pF
C1097	2113741F25	CAP1n
C1098	2113741F25	CAP1n
C1099	2113741F33	CAP 2200pF
C1100	2113741F33	CAP 2200pF
C1101	2113740F51	CAP100pF
C1102	2113740F51	CAP100pF
C1103	2113741A57	CAP 33n
C1104	2113743E07	CAP.022uF

Circuit Ref.	Motorola Part No.	Description
C1105	2113740F67	CAP 470p
C1106	2113740F67	CAP 470p
C1107	2113740F67	CAP 470p
C1108	2113740A67	CAP 330pF
C1110	2113740F55	CAP150pF
C1113	2113740F59	CAP 220pF
C1114	2113740F59	CAP 220pF
C1115	2113740F59	CAP 220pF
C1116	2113740F59	CAP 220pF
C1119	2113741F25	CAP1000pF
C1121	2113740F43	CAP 47pF
C1122	NOT PLACED	CAP 220pF
C1123	NOT PLACED	CAP 220pF
C1124	NOT PLACED	CAP 220pF
C1125	NOT PLACED	CAP 220pF
C1126	NOT PLACED	CAP 220pF
C1127	2113741F25	CAP1000pF
C1128	2113741F25	CAP1000pF
C1129	NOT PLACED	CAP 2200pF
C1130	2113741F33	CAP 2200pF
C1131	2113741F33	CAP 2200pF
C1132	2113741F33	CAP 2200pF
C1133	2113741F33	CAP 2200pF
C1135	NOT PLACED	CAP 1000pF
C1501	2113740F62	CAP 300pF
C1502	NOT PLACED	CAP 470pF
C1503	2111078B48	CAP160pF
C1504	NOT PLACED	CAP 270pF
C1505	NOT PLACED	CAP160pF
C1506	2113740F60	CAP 240pF

Circuit Ref.	Motorola Part No.	Description
C1507	2113741F33	CAP 2200pF
C1508	2111078B47	CAP150pF
C1509	2111078B47	CAP150pF
C1510	2111078B21	CAP 20pF
C1511	NOT PLACED	CAP 270pF
C1513	2111078B36	CAP 56pF
C1514	NOT PLACED	CAP 240pF
C1515	NOT PLACED	CAP 20pF
C1516	2111078B37	CAP 62pF
C1517	NOT PLACED	CAP16pF
C1518	NOT PLACED	CAP16pF
C1519	2111078B47	CAP150pF
C1520	NOT PLACED	CAP 470pF
C1521	2111078B34	CAP 47pF
C1522	2111078B38	CAP 68pF
C1523	2111078B39	CAP 75pF
C1524	NOT PLACED	CAP 43pF
C1525	NOT PLACED	CAP 51pF
C1526	NOT PLACED	CAP 43pF
C1527	NOT PLACED	CAP 43pF
C1528	2111078B34	CAP 47pF
C1529	NOT PLACED	CAP 43pF
C1530	2111078B49	CAP180pF
C1531	2111078B52	CAP 240pF
C1532	2111078B18	CAP15pF
C1534	NOT PLACED	CAP 27pF
C1535	NOT PLACED	CAP 39pF
C1536	2113741F33	CAP 2200pF
C1537	2111078B34	CAP 47pF
C1538	2111078B16	CAP13pF

Circuit Ref.	Motorola Part No.	Description
C1539	2111078B05	CAP 4.7pF
C1540	2113740F39	CAP 33pF
C1541	2113740F39	CAP 33pF
C1542	NOT PLACED	CAP 8.2pF
C2001	2311049J11	CAPP 4.7uF
C2002	2311049A56	CAPP 4.7uF
C2004	2113743F18	CAP 2.2uF
C2005	2113743F18	CAP 2.2uF
C2006	2113743F18	CAP 2.2uF
C2013	2113743E20	CAP 0.1uF
C2014	2113743E20	CAP 0.1uF
C2015	2113743E20	CAP 0.1uF
C2016	2113743E20	CAP 0.1uF
C2017	2113743E20	CAP 0.1uF
C2020	2113743K15	CAP 0.1uF
C2023	2113741F49	CAP 10n
C2024	2113741F49	CAP 10n
C2025	2113741F49	CAP 10n
C2026	2113741F49	CAP 10n
C2027	2113741F49	CAP 10n
C2028	2113743E20	CAP 0.1uF
C2033	2113741F25	CAP1n
C2034	2113741F33	CAP 2200pF
C2035	2113741F33	CAP 2200pF
C2036	2113741F25	CAP1n
C2037	NOT PLACED	CAP 2200pF
C2045	2113740F59	CAP 220pF
C2046	2113740F59	CAP 220pF
C2047	2113740F59	CAP 220pF
C2048	2113740F59	CAP 220pF

Circuit Ref.	Motorola Part No.	Description
C2049	NOT PLACED	CAP 1000pF
C2050	2113741F25	CAP 1000pF
C2051	2113740F54	CAP130pF
C2053	2113740F51	CAP100p
C2054	2113740F45	CAP 56pF
C2055	2113740F35	CAP 22p
C2072	NOT PLACED	CAP 2.7p
C2074	2113743E20	CAP 0.1uF
C2076	NOT PLACED	CAP 0.1uF
C2077	NOT PLACED	CAP DNF
C2078	0886629Z02	CAP 1uF
C2079	NOT PLACED	CAP DNF
C2072B	2113740F21	CAP 5.6pF
C2080	NOT PLACED	CAP 180pF
C2201	NOT PLACED	CAP 4.7pF
C2202	2113740F34	CAP 20pF
C2205	2113740F45	CAP 56pF
C2206	NOT PLACED	CAP 20pF
C2207	2113740F34	CAP 20pF
C2209	2113740F38	CAP 30pF
C2210	2113740F45	CAP 56pF
C2211	NOT PLACED	CAP 10pF
C2300	2113741F37	CAP 3300pF
C2301	2113740F27	CAP 10pF
C2302	2113740F35	CAP 22pF
C2304	2113740F59	CAP 220pF
C2305	2113740F57	CAP 180pF
C2306	NOT PLACED	CAP 27pF
C2307	2113741F37	CAP 3300pF
C2308	2113741F25	CAP 1000pF

Circuit Ref.	Motorola Part No.	Description
C2309	2113741F13	CAP 330pF
C2310	2113741F13	CAP 330pF
C2311	2113741F37	CAP 3300pF
C2312	2113741F25	CAP 1000pF
C2313	2113740F51	CAP 100pF
C2314	2113740F35	CAP 22pF
C2315	2113740F59	CAP 220pF
C2316	2113740F57	CAP 180pF
C2317	NOT PLACED	CAP 27pF
C2318	NOT PLACED	CAP 4.7pF
C2319	2113741F25	CAP 1000pF
C2320	2113741F25	CAP 1000pF
C2321	NOT PLACED	CAP 100pF
C2322	2113741F49	CAP .01uF
C2323	2113740F34	CAP 20pF
C2324	2113740F34	CAP 20pF
C2325	2113740F39	CAP 33pF
C2326	2113740F39	CAP 33pF
C2327	2113740F51	CAP 100pF
C2328	NOT PLACED	CAP 100pF
C2329	NOT PLACED	CAP 100pF
C2330	2113741F37	CAP 3300pF
C2335	NOT PLACED	CAP 100pF
C2336	NOT PLACED	CAP 100pF
C2337	2113741F37	CAP 3300pF
C2338	2113740F49	CAP 82pF
C2722	2113743A31	CAP 1uF
C2731	2113741F25	CAP 1000pF
C2732	NOT PLACED	CAP 1pF
C2733	2113740F31	CAP 15pF

Circuit Ref.	Motorola Part No.	Description
C2734	2113740F13	CAP 2.7pF
C2735	2113741F17	CAP 470pF
C2736	2113740F51	CAP 100pF
C2737	2113740F51	CAP 100pF
C2738	2113740F42	CAP 43pF
C2739	2113740F33	CAP 18pF
C2740	2113740F36	CAP 24pF
C2741	NOT PLACED	CAP 47pF
C2743	2113743E20	CAP 0.1uF
C2744	2113741F25	CAP 1000pF
C2745	2113741F25	CAP 1000pF
C2750	NOT PLACED	CAP .01uF
C2751	2113741F49	CAP .01uF
C2752	2113740F42	CAP 43pF
C2753	2113740F42	CAP 43pF
C2754	2113740F37	CAP 27pF
C2755	2113740F27	CAP 10pF
C2756	2113740F27	CAP 10pF
C2757	2113741F25	CAP 1000pF
C2758	2113741F25	CAP 1000pF
C2761	2113740F31	CAP 15pF
C2762	2113740F31	CAP 15pF
C2763	2113741F49	CAP .01uF
C2764	2113740F21	CAP 5.6pF
C2765	2113740F38	CAP 30pF
C2766	2113740F51	CAP 100pF
C2767	2113741F49	CAP .01uF
C2771	2113743E20	CAP 0.1uF
C2772	2113741F25	CAP 1000pF
C2773	NOT PLACED	CAP 4.7pF

Circuit Ref.	Motorola Part No.	Description
C2775	2113740F37	CAP 27pF
C2776	2113740F47	CAP 68pF
C2777	2113740F37	CAP 27pF
C2778	2113740F43	CAP 47pF
C2779	2113741F17	CAP 470pF
C2780	2113743E20	CAP 0.1uF
C2781	2113741F49	CAP .01uF
C2782	2113741F25	CAP 1000pF
C2784	2113740F19	CAP 4.7pF
C2785	2113740F39	CAP 33pF
C2790	2113740F29	CAP 12pF
C2791	2113741F49	CAP .01uF
C2792	2113743E20	CAP 0.1uF
C2793	2113741F49	CA .01uF
C2794	2113740F24	CAP 7.5pF
C2795	2113740F23	CAP .8pF
C2796	2113741F49	CAP VALUE
C2805	2113743E20	CA 0.1uF
C2806	2113741F25	CAP 1000pF
C5000	2113741F25	CAP 1000pF
C5001	2380090M24	CAPP 10uF
C5002	2311049A99	CAPP 47uF
C5003	2311049A99	CAPP 47uF
C5005	2311049A97	CAPP 33uF
C5006	2311049A57	CAPP 10uF
C5007	2311049A57	CAPP 10uF
C5008	2311049A57	CAPP 10uF
C5009	2311049A57	CAPP 10uF
C5010	2311049A57	CAPP 10uF
C5011	2311049A57	CAPP 10uF

Circuit Ref.	Motorola Part No.	Description
C5012	2311049A56	CAPP 4.7u
C5013	2113928P04	CAP 1u
C5014	NOT PLACED	CAP 2.2uF
C5015	NOT PLACED	CAP 0.1uF
C5016	NOT PLACED	CAP 0.1uF
C5017	NOT PLACED	CAP 0.1uF
C5018	NOT PLACED	CAP 0.1uF
C5019	2113743K15	CAP 0.1uF
C5020	2113743K15	CAP 0.1uF
C5021	2113743K15	CAP 0.1uF
C5022	2113743K15	CAP 0.1uF
C5023	2113743K15	CAP 0.1uF
C5024	2113743K15	CAP 0.1uF
C5025	2113743K15	CAP 0.1uF
C5026	2113743K15	CAP 0.1uF
C5027	2113743K15	CAP 0.1uF
C5028	2113743K15	CAP 0.1uF
C5029	2113743K15	CAP 0.1uF
C5030	2113743K15	CAP 0.1uF
C5031	2113743K15	CAP 0.1uF
C5032	2113743K15	CAP 0.1uF
C5033	2113743K15	CAP 0.1uF
C5034	2113743K15	CAP 0.1uF
C5035	2113743K15	CAP100n
C5036	2113743K15	CAP 0.1uF
C5037	2113743K15	CAP 0.1uF
C5038	2113743K15	CAP 100n
C5039	NOT PLACED	CAP 100n
C5040	NOT PLACED	CAP 100n
C5041	2113743F18	CAP 2.2uF

Circuit Ref.	Motorola Part No.	Description
C5042	2113743F16	CAP 1u
C5043	2113743F16	CAP 1u
C5044	2113743F16	CAP 1u
C5045	2113743F16	CAP 1uF
C5046	2113743E20	CAP 0.1uF
C5047	2113743E20	CAP 0.1uF
C5048	2113743E20	CAP 0.1uF
C5049	2113743E20	CAP 0.1uF
C5050	2113743E20	CAP 0.1uF
C5051	2113743E20	CAP 0.1uF (CM360)
C5052	2113743E20	CAP 0.1uF
C5053	2113743E20	CAP 0.1uF (CM360)
C5054	2113743E20	CAP 0.1uF (CM360)
C5055	2113741M69	CAP 0.1uF
C5056	2113741M69	CAP 0.1uF (CM360)
C5057	2113743E20	CAP 0.1uF
C5058	NOT PLACED	CAP 0.1uF
C5059	2113743E07	CAP .022uF
C5060	2113743K15	CAP 100n
C5061	2113741M69	CAP 0.1uF
C5062	2113741M69	CAP 0.1uF
C5063	2113741M69	CAP 0.1uF
C5064	NOT PLACED	CAP1000pF
C5065	NOTPLACED	CAP 1000pF
C5066	NOT PLACED	CAP 1000pF
C5067	2113741F25	CAP 1000pF
C5068	NOT PLACED	CAP 1000pF
C5069	NOT PLACED	CAP 1000pF
C5070	NOT PLACED	CAP 1000pF
C5071	2113741F25	CAP 1000pF

Circuit Ref.	Motorola Part No.	Description
C5072	2113741F25	CAP 1000pF
C5073	2113741F25	CAP 1000pF
C5074	NOT PLACED	CAP 1000pF
C5075	NOT PLACED	CAP 1000pF
C5076	2113741F25	CAP 1000pF
C5077	2113741F25	CAP 1000pF
C5078	2113741F25	CAP 1000pF
C5079	2113741F25	CAP 1000pF
C5080	2113741F25	CAP 1000pF
C5081	2113741F25	CAP 1000pF
C5082	2113741F25	CAP 1000pF
C5083	2113740F51	CAP 100pF
C5084	2113740F51	CAP 100pF
C5085	2113741A53	CAP .022uF
C5086	2113741A53	CAP .022uF
C5087	2113740F49	CAP 82p
C5088	2113740F49	CAP 82pF
C5089	NOT PLACED	CAP 82pF
C5090	2113740F49	CAP 82p
C5091	2113740F49	CAP 82pF
C5092	NOT PLACED	CAP 220pF
C5094	NOT PLACED	CAP 220pF
C5095	NOT PLACED	CAP 220pF
C5096	NOT PLACED	CAP 220pF
C5097	2113740F59	CAP 220pF
C5098	2113740F59	CAP 220pF
C5099	2113740F59	CAP 220pF
C5100	2113740F59	CAP 220pF
C5101	2113741F25	CAP 1000pF (CM360)
C5102	2113743E20	CAP 0.1uF (CM360)

Circuit Ref.	Motorola Part No.	Description
C5103	2113743K15	CAP100n (CM360)
C5104	2113741F25	CAP 1000pF
C5110	2113741F25	CAP 1000pF
C5111	2113741F25	CAP 1000pF
C5119	2113743H14	CAP 10uF
C5120	2311049A99	CAPP 47uF
C5555	2113741A45	CAP .01uF
C5559	2113741F25	CAP 1000pF
C5560	2113741F33	CAP 2200pF
D1	4880142L01	MMBV3401LT
D3	4802245J97	DAN235ETL
D4	4802245J97	DAN235ETL
D5	4802245J97	DAN235ETL
D6	4802245J97	DAN235ETL
D100	NOT PLACED	MMBD6100
D101	4813833C02	MMBD6100
D102	4813833C02	MMBD6100
D103	4802482J02	MA4P959
D104	4802482J02	MA4P959
D105	4805218N57	RB715F
D106	4805218N57	RB715F
D107	4805218N57	RB715F
D108	4805218N57	RB715F
D200	4802233J09	IMN10
D201	4802233J09	IMN10
D202	NOT PLACED	1SV232
D202B	4862824C03	1SV232
D400	4813833C07	MMBD7000
D401	4813833C02	MMBD6100
D402	NOT PLACED	RB751V40

Circuit Ref.	Motorola Part No.	Description
D500	4813833C02	MMBD6100
D501	4813833C02	MMBD6100
D502	4813825A23	MMSD301T1
D513	4813833C02	MMBD6100
D2201	4880154K03	MMBD353
D2301	4805649Q13	1SV228
D2303	4880154K03	MMBD353
D2304	4805649Q13	1SV228
D2731	4805649Q13	1SV228
D2732	4805649Q13	1SV228
D2733	4805649Q13	1SV228
D2739	4813825A05	MMBD301
D2751	4805649Q13	1SV228
D2752	4805649Q13	1SV228
D2754	4813825A05	MMBD301
FL2	9180468V06	FLTR
FL3	9180468V04	FLTR
FL4	9180469V03	CFWC455G
FL5	9180469V06	CFWC455D
FL2201	9166509A01	TS2-21B01
FL2202	9166509A01	TS2-21B01
J1	2889309U01	CONN_P
J2	0989241U02	CONN_J 20 PIN
J3	0986615Z01	CONN 28PIN ZIF (CM360)
L1	2462587M23	IDCTR 2.7uH
L2	2462587N69	IDCTR 1.2uH
L3	2462587N69	IDCTR 1.2uH
L6	2462587N69	IDCTR 1.2uH
L13	2462587N53	IDCTR 100nH

Circuit Ref.	Motorola Part No.	Description
L14	2462587N53	IDCTR 100nH
L16	NOT PLACED	IDCTR 27nH
L100	2484657R01	57R01
L101	2462587T30	IDCTR 1uH
L102	2462587T30	IDCTR 1uH
L103	2462587T30	IDCTR 1uH
L104	2462587N64	IDCTR 680nH
L105	2462587N55	IDCTR 150nH
L107	2409377M03	IDCTR 6.8nH
L108	2462587N69	IDCTR 1.2uH
L115	2485873L09	IDCTR 38.13nH
L117	2484657R01	57R01
L118	2484657R01	57R01
L119	2484657R01	57R01
L120	2484657R01	57R01
L121	2484657R01	57R01
L122	2408384A10	IDCTR 120nH
L200	2462587Q46	IDCTR 820nH
L205	2462587Q47	IDCTR1uH
L217	2462587Q46	IDCTR 820nH
L500	2484657R01	57R01
L501	2484657R01	57R01 0n
L502	2484657R01	57R01 0n
L1502	2460591E64	IDCTR 30.51nH
L1503	2460591A11	IDCTR 7.66nH
L1504	2460591L29	IDCTR 16.03nH
L1505	2485873L09	IDCTR 38.13nH
L1507	2462587T12	IDCTR 56nH
L1511	2485873L12	IDCTR 71.5nH
L1512	2485873L12	IDCTR 71.5nH

Circuit Ref.	Motorola Part No.	Description
L1513	2485873L12	IDCTR 71.5nH
L1514	2485873L12	IDCTR 71.5nH
L1515	2485873L12	IDCTR 71.5nH
L1518	NOT PLACED	IDCTR 1.2uH
L1519	2462587N56	IDCTR 180nH
L2201	2462587M23	IDCTR 2.7uH
L2202	NOT PLACED	IDCTR 2.7uH
L2203	2462587M23	IDCTR 2.7uH
L2302	2462587T23	IDCTR 470nH
L2731	2462587N58	IDCTR 270nH
L2732	2462587N68	IDCTR 1uH
L2733	2462587T23	IDCTR 470nH
L2734	2462587T16	IDCTR 120nH
L2741	2462587N68	IDCTR 1uH
L2742	2462587N68	IDCTR 1uH
L2750	2462587T30	IDCTR 1uH
L2751	2462587N68	IDCTR 1uH
L2752	2462587T18	IDCTR 180nH
L2753	2462587T18	IDCTR 180nH
L2754	2462587N68	IDCTR 1uH
L2761	2462587N55	IDCTR150nH
L2768	2462587N54	IDCTR 120nH
L2774	2462587N50	IDCTR 56nH
L2775	2462587N50	IDCTR 56nH
L2781	2462587N56	IDCTR 180nH
L2790	2462587N56	IDCTR 180nH
L2792	2462587N69	IDCTR 1.2uH
M9	0289511U01	NUT
M100	NOT PLACED	DRV_CLIP
M101	NOT PLACED	CONTACT

Circuit Ref.	Motorola Part No.	Description
M102	NOT PLACED	CONTACT
M103	NOT PLACED	CONTACT
M104	NOT PLACED	CONTACT
M105	2680499Z01	HEATSINK
M201	7588823L03	CONTACT
M202	7588823L03	CONTACT
M203	7588823L03	CONTACT
M204	7588823L04	CONTACT
M205	7588823L04	CONTACT
M206	7588823L04	CONTACT
PCB	8489012U01	
P1	2804503J01	CONN_P
P2	NOT PLACED	CONN_P
Q1	4809939C04	UMC3
Q3	4813824A10	MMBT3904
Q4	4809939C04	UMC3
Q6	4802197J95	PBR941
Q100	4886136B01	MRF1550
Q101	4809940E02	DTC114YE
Q102	4809940E02	DTC114YE
Q103	4813824A06	MMBTA13
Q104	4813824A10	MMBT3904
Q105	4813828A08	MRF1511
Q106	4805128M27	BSR33
Q107	4809940E02	DTC114YE
Q108	NOT PLACED	MMBT3904
Q109	4813824A10	MMBT3904
Q110	4809940E02	DTC114YE
Q400	4809940E02	DTC114YE
Q401	4880141L03	BCW68G

Circuit Ref.	Motorola Part No.	Description
Q403	4809940E02	DTC114YE
Q404	4809940E02	DTC114YE
Q405	4809940E02	DTC114YE
Q407	4809940E02	DTC114YE
Q408	4880048M01	DTC144EKA
Q409	4880048M01	DTC144EKA
Q410	4880048M01	DTC144EKA
Q411	4880048M01	DTC144EKA
Q412	4880048M01	DTC144EKA
Q413	4809940E02	DTC114YE
Q414	4809940E02	DTC114YE
Q415	NOT PLACED	MMBT3904
Q417	4813824A10	MMBT3904
Q500	4813824A65	MMBT3904WT1
Q501	4809940E02	DTC114YE
Q502	4809940E02	DTC114YE
Q503	4813824A65	MMBT3904WT1
Q504	4880048M01	DTC144EKA
Q505	4813824A10	MMBT3904
Q506	4813824A10	MMBT3904
Q507	NOTPLACED	DTC114YE
Q514	4802393L66	SI3455ADV
Q2301	4802197J95	PBR941
Q2302	4813824A17	MMBT3906
Q2741	4813823A05	MMBFU310L
Q2742	4805921T09	FMG8A
Q2751	4813823A05	MMBFU310L
Q2752	4813824A10	MMBT3904
Q2760	4802197J95	PBR941
Q2770	4802197J95	PBR941

Circuit Ref.	Motorola Part No.	Description
Q2780	4802197J95	PBR941
Q2790	4802197J95	PBR941
Q2791	4809939C04	UMC3
R1	0662057A40	RES 430
R2	0662057A41	RES 470
R4	0662057B47	RES 0.
R5	0662057A82	RES 24K
R6	0662057A80	RES 20.K
R7	0662057A80	RES 20.K
R8	0662057A80	RES 20.K
R9	0662057A80	RES 20.K
R10	0662057A77	RES15.K
R12	NOT PLACED	RES 15.K
R13	0662057A73	RES 10K
R14	0662057A75	RES 12.K
R15	0662057A75	RES 12.K
R16	0662057A75	RES 12.K
R17	0662057A75	RES 12.K
R18	0662057A75	RES 12.K
R19	0662057A75	RES 12.K
R20	0662057A75	RES 12.K
R21	0662057A73	RES 10K
R23	0662057A71	RES 8.2K
R24	0662057A69	RES 6.8K
R25	0662057A65	RES 4.7K
R26	0662057A61	RES 3.3K
R27	0662057A61	RES 3.3K
R28	0662057A58	RES 2.4K
R30	0662057A55	RES 1.8K
R31	0662057A51	RES 1.2K

Circuit Ref.	Motorola Part No.	Description
R33	0662057A45	RES 680.
R34	0662057A59	RES 2.7K
R35	0662057A39	RES 390.
R36	NOT PLACED	RES 0
R37	0662057A25	RES 100.
R38	0662057A33	RES 220
R39	0662057A18	RES 51.
R41	0662057A18	RES 51.
R100	NOT PLACED	RES 39K
R101	1705603W01	SHUNT 1.639m
R102	0683962T51	RES 120
R103	0683962T51	RES 120
R104	0683962T51	RES 120
R105	0680194M18	RES 51.0
R106	0680194M18	RES 51.0
R107	0680194M18	RES 51.000
R108	0680194M18	RES 51.000
R109	0662057A15	RES 39
R110	0662057P10	RES 10K
R111	0662057P10	RES 10K
R112	0662057T21	RES 332K
R113	0662057P10	RES 10.K
R114	0662057P10	RES 10.K
R115	0662057P10	RES 10.K
R116	0662057P10	RES 10.K
R117	0662057A77	RES 15K
R118	0662057A45	RES 680
R119	0662057A29	RES 150
R120	0662057A45	RES 680
R121	0662057A29	RES 150

Circuit Ref.	Motorola Part No.	Description
R122	0662057C19	RES 4.7
R123	0662057C13	RES 2.7
R124	0662057C13	RES 2.7
R125	0662057C13	RES 2.7
R126	0662057C03	RES 1
R127	0662057C03	RES 1
R130	0662057B47	RES 0
R131	0662057A73	RES 10K
R132	0662057T38	RES 750K
R134	0662057A65	RES 4.7K
R135	0662057A88	RES 43K
R136	0662057A87	RES 39.K
R137	0662057A87	RES 39.K
R138	0662057A89	RES 47K
R139	0662057A89	RES 47K
R140	0662057A81	RES 22K
R141	0662057A81	RES 22.K
R142	0662057A81	RES 22.K
R143	0662057A81	RES 22.K
R144	0662057A81	RES 22K
R145	0662057A81	RES 22K
R146	0662057A81	RES 22.K
R147	0662057A81	RES 22K
R148	0662057A81	RES 22.K
R149	0662057A81	RES 22.K
R151	0662057A69	RES 6.8K
R152	0662057C99	RES 10K
R156	0662057A73	RES 10.K
R157	0662057A91	RES 56K
R158	0662057A67	RES 5.6K

Circuit Ref.	Motorola Part No.	Description
R159	0662057A67	RES5.6K
R160	0662057A61	RES 3.3K
R161	0662057A61	RES 3.3K
R162	0662057A61	RES 3.3K
R163	0662057A61	RES 3.3K
R164	0662057A74	RES 11K
R165	0662057A58	RES 2.4K
R166	0662057A58	RES 2.4K
R167	0662057A57	RES 2.2K
R168	0662057A57	RES 2.2K
R169	0662057A57	RES 2.2K
R170	0662057A42	RES 510.
R171	0662057A41	RES 470
R172	0662057A41	RES 470.
R173	0662057A29	RES 150
R174	0662057A29	RES 150
R175	0662057A33	RES 220
R176	0662057A25	RES 100
R177	NOT PLACED	RES 22K
R178	0662057A25	RES 100
R179	NOT PLACED	RES 36.
R180	0662057A89	RES 47K
R181	0662057A89	RES 47K
R182	0662057B47	RES 0
R183	NOT PLACED	RES 47K
R185	0662057A73	RES 10K
R186	NOT PLACED	RES 0
R187	NOT PLACED	RES 0
R188	NOT PLACED	RES 0
R189	0662057A61	RES 3.3K

Circuit Ref.	Motorola Part No.	Description
R190	0662057B47	RES 0
R191	0662057A73	RES 10K
R192	0662057A61	RES 3.3K
R193	0662057A73	RES 10K
R194	0662057A86	RES 36K
R195	0662057A73	RES 10K
R196	NOT PLACED	RES 3.3K
R197	NOT PLACED	RES 10K
R198	NOT PLACED	RES 100K
R199	NOT PLACED	RES 0
R200	0662057B07	RES 240K
R201	0662057A73	RES 10K
R202	NOT PLACED	RES 0.
R204	NOT PLACED	RES 0
R205	NOT PLACED	RES 0
R206	0662057B02	RES 150K
R207	NOT PLACED	RES 150.K
R209	0662057A97	RES 100.K
R207B	0662057B02	RES 150.K
R210	0662057A97	RES 100.K
R217	0662057A43	RES 560
R224	0662057A41	RES 470
R225	0662057A29	RES 150.
R226	0662057A29	RES 150.
R228	0662057A25	RES 100.
R229	0662057A25	RES 100.
R234	0662057A25	RES 100
R235	NOT PLACED	RES 0
R401	0662057C85	RES 2.7K
R402	0662057B47	RES 0.

Circuit Ref.	Motorola Part No.	Description
R403	0662057B47	RES 0.
R404	0662057B47	RES 0.
R405	0662057B47	RES 0.
R406	0662057B47	RES 0.
R407	0662057B47	RES 0.
R414	0662057B47	RES 0.
R415	0662057B47	RES 0.
R421	0662057B47	RES 0
R422	NOT PLACED	RES10K
R423	NOT PLACED	RES 100.K
R424	NOT PLACED	RES 100.K
R425	0662057A97	RES 100.K
R426	NOT PLACED	RES 100.K
R427	NOT PLACED	RES 100.K
R428	0662057A97	RES 100.K
R429	0662057A97	RES 100K
R430	0662057A87	RES 39K
R431	NOT PLACED	RES 10K
R432	0662057A85	RES 33.K
R433	0662057A85	RES 33.K
R434	0662057A85	RES 33.K
R435	0662057A85	RES 33.K
R436	0662057A85	RES 33.K
R438	0662057A73	RES 10.K
R439	0662057A73	RES 10.K
R440	0662057A73	RES 10.K
R441	0662057A73	RES 10.K
R442	0662057A73	RES 10.K
R443	0662057A61	RES 3.3K
R444	0662057A73	RES 10.K

Circuit Ref.	Motorola Part No.	Description
R445	0662057A73	RES 10.K
R447	0662057A01	RES 10
R450	0662057A73	RES 10.K
R451	0662057A73	RES 10.K
R453	0662057A61	RES 3.3K
R454	0662057A61	RES 3.3K
R455	0662057A61	RES 3.3K
R456	0662057A61	RES 3.3K
R457	0662057A61	RES 3.3K
R458	0662057A61	RES 3.3K
R459	NOT PLACED	RES 47K
R460	0662057A53	RES 1.5K
R461	0662057A33	RES 220
R462	0662057A18	RES 51
R463	0662057A73	RES 10K
R466	NOT PLACED	RES 0
R467	NOT PLACED	RES 0
R468	NOT PLACED	RES 0
R469	NOT PLACED	RES 0
R470	0662057A73	RES 10.K
R472	NOT PLACED	RES 100K
R473	NOT PLACED	RES 100K
R600	0662057C01	RES 0
R601	0611077A62	RES 330
R610	0662057C59	RES 220
R611	NOT PLACED	RES 0
R612	0662057C01	RES 0
R613	0662057C01	RES 0
R692	0662057A87	RES 39K
R693	0662057A87	RES 39K

Circuit Ref.	Motorola Part No.	Description
R694	0662057A97	RES 100K
R1502	0662057B47	RES 0
R1503	0662057A01	RES 10
R1506	0662057A01	RES 10
R1507	0611077A01	RES 0
R2301	0662057A97	RES 100K
R2302	0662057A37	RES 330
R2303	0662057A49	RES 1K
R2304	0662057A53	RES 1.5K
R2305	NOT PLACED	RES 10K
R2306	0662057A35	RES 270
R2307	0662057A21	RES 68
R2308	0662057A35	RES 270
R2309	0662057A97	RES 100K
R2311	0662057A63	RES 3.9K
R2312	0662057A59	RES 2.7K
R2313	0662057A61	RES 3.3K
R2314	0662057B67	RES 6.2
R2316	0662057A29	RES 150
R2317	0662057A29	RES 150
R2318	0662057A13	RES 33
R2321	2113740F29	RES 12pF
R2714	0662057B02	RES 150K
R2731	0662057A13	RES 33
R2739	0662057A83	RES 27K
R2740	0662057A09	RES 22
R2741	0662057A21	RES 68
R2742	0662057A15	RES 39
R2743	0662057A65	RES 4.7K
R2751	0662057A83	RES 27K

Circuit Ref.	Motorola Part No.	Description
R2752	0662057A57	RES 2.2K
R2753	0662057A21	RES 68
R2754	0662057A15	RES 39
R2758	0662057A25	RES 100
R2760	0662057B47	RES 0
R2761	0662057A55	RES 1.8K
R2762	0662057A41	RES 470
R2763	0662057A25	RES 100
R2765	0662057A29	RES 150
R2766	0662057A15	RES 39
R2767	0662057A29	RES 150
R2768	0662057A59	RES 2.7K
R2769	0662057A49	RES 1K
R2770	0662057A01	RES 10
R2771	0662057A29	RES 150
R2772	0662057A25	RES 100
R2773	0662057A35	RES 270
R2774	0662057A01	RES 10
R2775	NOT PLACED	RES 270
R2776	0662057A25	RES 100
R2777	0662057A35	RES 270
R2778	0662057A59	RES 2.7K
R2779	0662057A53	RES 1.5K
R2781	0662057A25	RES 100
R2782	0662057A25	RES 100
R2783	NOT PLACED	RES 10
R2784	0662057A01	RES 10
R2785	0662057A15	RES 39
R2786	0662057A29	RES 150
R2788	0662057A29	RES 150

Circuit Ref.	Motorola Part No.	Description
R2790	0662057B47	RES 0
R2791	0662057A41	RES 470
R2792	0662057A49	RES 1K
R2793	NOT PLACED	RES 1K
R2794	0662057A18	RES 51
R2795	0662057A49	RES 1K
R2796	0662057A35	RES VALUE
R2797	NOT PLACED	RES 0
R2808	0662057A01	RES 10
R2810	NOT PLACED	RES 470
R2811	0662057A97	RES 100K
R5000	0662057B47	RES 0
R5001	0662057T68	RES 1K
R5002	0662057B47	RES 0 (CM360)
R5006	0662057B47	RES 0
R5007	0662057A89	RES 47K
R5008	0662057B47	RES 0
R5009	0662057B47	RES 0
R5010	0662057B47	RES 0
R5011	NOT PLACED	RES 0
R5013	NOT PLACED	RES 0
R5014	0662057B47	RES 0
R5019	0662057B08	RES 270.K
R5020	0662057B02	RES 150K
R5021	0662057A97	RES 100K
R5022	0662057A97	RES 100K
R5023	0662057A97	RES 100K
R5024	0662057A97	RES 100K (CM360)
R5025	0662057A97	RES 100K
R5026	0662057A85	RES 33K

Circuit Ref.	Motorola Part No.	Description
R5027	0662057B08	RES 270K
R5028	0662057A97	RES 100K
R5029	0662057A97	RES 100K
R5030	0662057A85	RES 33K
R5031	0662057A92	RES 62K
R5032	0662057A91	RES 56.K
R5033	0662057A89	RES 47K
R5034	0662057A89	RES 47K
R5035	0662057A89	RES 47K
R5036	0662057A89	RES 47K
R5037	0662057A73	RES 10K
R5038	0662057A85	RES 33K
R5039	0662057A97	RES 100K
R5040	0662057A84	RES 30.K
R5041	0662057A82	RES 24K
R5042	0662057A82	RES 24K
R5043	0662057A82	RES 24K
R5044	0662057A82	RES 24K
R5045	0662057A85	RES 33K
R5046	0662057A82	RES 24K
R5047	0662057B47	RES 0 (CM340)
R5048	0662057A82	RES 24K
R5049	0662057A77	RES 15K
R5050	0662057A76	RES 13K
R5051	0662057A75	RES 12K
R5052	0662057A73	RES 10K
R5053	0662057A73	RES 10K
R5054	0662057A73	RES 10K
R5055	0662057A73	RES 10K
R5056	0662057A73	RES 10K

Circuit Ref.	Motorola Part No.	Description
R5057	0662057A73	RES 10K
R5058	NOT PLACED	RES 10K
R5059	NOT PLACED	RES 10K
R5060	0662057A73	RES 10K
R5061	0662057A73	RES 10K
R5062	0662057A73	RES 10K
R5063	NOT PLACED	RES 8.2K
R5064	NOT PLACED	RES 8.2K
R5065	0662057A68	RES 6.2K
R5066	0662057A68	RES 6.2K
R5067	NOT PLACED	RES 6.2K
R5068	NOT PLACED	RES 6.2K
R5069	0662057A73	RES 10K
R5070	0662057A57	RES 2.2K
R5071	0662057A57	RES 2.2K
R5072	0662057A65	RES 4.7K
R5073	0662057A49	RES 1K
R5074	0662057A49	RES 1K
R5075	0662057A42	RES 510.
R5076	0662057A42	RES 510.
R5077	0662057A36	RES 300
R5078	0662057A25	RES 100.
R5079	0662057A25	RES 100.
R5080	0662057A01	RES 10.
R5081	0613952D78	RES 6.34K
R5082	0662057A90	RES 51K
R5083	0662057B08	RES 270K
R5084	0662057B47	RES 0 (CM360)
R5085	NOT PLACED	RES 1MEG
R5089	NOT PLACED	RES 1MEG

Circuit Ref.	Motorola Part No.	Description
R5091	0662057A43	RES 560
R5092	0662057A97	RES 100K
R5103	0662057A82	RES 24K
RT100	0680361L01	THERM 47K
S5010	1889288U01	SWITCH
SH1	2602023X12	shield
SH2	2602641Y02	shield
SH3	2602023X10	shield
SH4	2602023X10	shield
SH100	NOT PLACED	PA Shield
SH2301	2605915V01	SHIELD
SH2302	NOT PLACED	SHIELD
T1	2580541Z02	XFMR
T2	2580541Z02	XFMR
U1	4808612Y05	SMS3928_023
U2	5186144B01	SA616
U3	5109522E10	TC7W04F
U100	5113818A01	LM2904
U101	5185130C65	30C65
U102	5113818A01	LM2904
U103	5113819A04	MC3303
U200	5185963A27	63A27
U400	5102463J64	X25128-2.7
U401	4809940E02	DTC114YE
U402	5102463J36	SRM2B256
U403	5102226J56	MC68HC11FL0
U404	5189233U21	FLASH 4 MEG AT49LV040-70VI
U405	5113805A75	MC74HC595A
U501	0104016J81	LM2941T

Circuit Ref.	Motorola Part No.	Description
U502	5102463J95	TDA1519C
U503	5105469E65	LP2951C
U504	5185130C53	30C53
U505	5113818A01	LM2904
U506	5113818A01	LM2904
U507	5113818A01	LM2904
U508	5113816A30	MC33269D
U509	5184704M60	HEF4053B
U510	5104187K94	LP2986ILDY
U511	4813833C02	MMBD6100
U515	5162852A59	MAX4599EXT (CM360)
U517	5113818A01	LM2904
VR101	4813830A15	MMBZ5232B
VR102	4813830A15	MMBZ5232B
VR103	4813830A33	MMBZ5250B
VR104	4813830A33	MMBZ5250B
VR400	NOT PLACED	MMBZ5235B
VR401	4813830G12	MMSZ4687T1
VR402	4813830A09	MMBZ5226B
VR500	4813832C77	MR2835S
VR501	4813830A14	MMBZ5231B
VR502	4813830G09	MMSZ4684
VR503	4813830G09	MMSZ4684
VR504	4813830G09	MMSZ4684
VR692	4813830A75	MMBZ20VAL
VR693	4813830A77	MMBZ33VAL
VR694	4813830A75	MMBZ20VAL
VR695	4813830A77	MMBZ33VAL
VR696	4813830A75	MMBZ20VAL
VR697	4813830A75	MMBZ20VAL

Circuit Ref.	Motorola Part No.	Description
VR698	4813830A75	MMBZ20VAL
VR699	4813830A75	MMBZ20VAL
Y1	9186145B02	45B02
Y2	4866541A01	TSX-5
Y200	NOT PLACED	45J68
Y201	NOT PLACED	14R06
Y202	4880114R06	14R06